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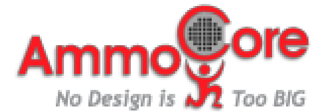

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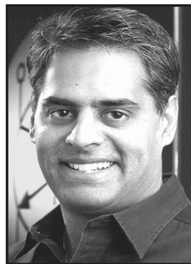
WELCOME

On behalf of the ISQED 2003 conference and technical committees, we are pleased to welcome you to the 4th International Symposium on Quality Electronic Design, ISQED 2003. Due to the overwhelming success of the first 3 conferences, despite the slump in the IC industry last year, and the unique value that it offers, IEEE ISQED is gaining recognition in both academia and industry. We look forward to continuing this tradition of excellence. All the technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 24-26 at the San Jose Double Tree Hotel. The hotel is located in the heart of Silicon Valley, near the San Jose International Airport, and is a very convenient location for all conference participants whether local, US or international attendees.

Ken Shepard
Program Chair

It is clear that advances in semiconductor processing and manufacturing technologies continue to progress at an ever increasing rate giving rise to complex processes and physics, and making possible increasingly complicated designs. Due to these advances, we have high levels of interdependency between integrated circuit design, semiconductor technology development, manufacturing, and test. In addition, issues of modeling, verification, validation and characterization have a critical role due to the highly complex interaction between IC design and process. Furthermore, evolving business models making possible the availability of IP from a variety of sources and where questions of qualification, use/reuse, and integration exacerbate this complexity. This program will attempt to address these issues by bringing together industry practitioners and academics engaged in deep sub-micron integrated circuit design and development. The technical sessions will span the numerous disciplines that in total define the IC industry, but whose common goal is the improvement of design quality, particularly with respect to metrics such as device robustness, yield, testability, design productivity and overall systems cost.



Bharath Rajagopalan
Conference Chair

Vivek De
Program Vice-Chair

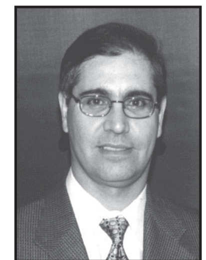
This conference provides a unique opportunity to bring together people and ideas to whose common goal understand and discuss the key issues faced by industry in the next few years, highlight emerging areas of importance, and provide possible solutions to these challenges.

Kaustav Banerjee
Conference Vice-Chair

The technical program for ISQED 2003 has been assembled by the technical program committee, which includes international experts from industry and academia. The technical program committee has selected papers for presentation from numerous excellent submissions. This year, a total of 39 papers were accepted for regular presentation from 119 papers submitted to ISQED 2003. Because of the high quality of this year's submissions, an additional 16 short papers were accepted. The technical program also includes nine invited papers from leading experts in the field. The ISQED 2003 Best Paper Award ceremony will be held during the plenary session on Tuesday.

Res Saleh
General Vice-Chair

The conference will commence with our popular tutorial sessions, organized by Tuna Tarim and Enrico Malavasi, and will be held on Monday, March 24. We will have four tracks, featuring experts from around the world. The tutorial sessions cover a variety of exciting and timely topics such as Test Methodologies for Quality Design, Testing and Yield of Integrated Circuits, IC and Package Co-design, and Design for Reliability. Topics to be presented includes: Testing and Yield of integrated circuits, Test structures for circuit yield assessment and modeling; Design based yield improvements (DBYI); Yield in flash memory - Methodology, modeling and design issues; Enhancing the Silicon-Package Interface Through Their Concurrent Design and Verification; A package design perspective - "It will be BGA and flip-chip"; An IC design perspective - "Why would we choose flip chip?"; Noise analysis for 0.13um and beyond; NBTI/HCI Modeling and Full-Chip Analysis in Design Environment; Overview of



Ali Iranmanesh
General Chair

WELCOME

with circuit design considerations. The 2003 tutorials at ISQED offer a truly outstanding opportunity to catch-up with the latest areas of research and development.

In keeping with our tradition of bringing highly renowned leaders from industry and academia to discuss vital issues from a macroscopic perspective, we are pleased to offer this year two plenary sessions, organized by Kris Verma and Lech Jozwiak. The first plenary session is on Tuesday and the second on Wednesday, with 3 speakers in each session. In the first keynote speech on Tuesday, entitled "Platform Leadership in the Ambient Intelligence Era", Bob Payne (CTO and Senior Vice President/GM of System ASIC Technology, Philips Semiconductors US), addresses several thought provoking issues related to the growing issues facing the SoC design methodology. Next, Susumu Kohyama (Corporate Senior Vice President, Toshiba Corporation) explores the inefficiency of the classic IDM model in his keynote speech entitled "Quality SoC Design and Implementation for Real Manufacturability". The presentation explores a "SoC centric Open IDM" perspective, where true knowledge of integration and management skill function to enhance differentiators on top of open platforms. The final speech by Ted Vucurevich (Senior Vice President and Chief Technical Office Cadence Design Systems, Inc.) is titled "Quality Challenges of the Nanometer Design Realm" where he elaborates on why at sub-nanometer levels, design-in across a design chain becomes a major bottleneck. He further promotes the notion of silicon-package-board co-design. On Wednesday, the first keynote speech will be entitled, "Addressing the IC Designer's Needs: Integrated Design Software for Faster, More Economical Chip Design", where Rajeev Madhavan (Chairman & CEO, Magma Design Automation) highlights the EDA industry's need to deliver integrated design flows that enable the design and production of chips with fewer resources and in less time, and without compromising the quality of results. Next, Michael Reinhardt (CEO & President, RubiCAD) explores the gap between ASIC and full-custom design and outlines possible strategies and practical solutions for achieving this closure. The final keynote speech is titled "A VLSI System Perspective for Microprocessors Beyond 90nm " and is presented Shekhar Borkar (Intel Fellow & Director of Circuit Research Lab). In this presentation, he explores the formidable obstacles of power delivery and dissipation toward continuous scaling of microprocessor designs and discusses potential solutions to overcome these barriers.

The ISQED 2003 program also includes three panels, one each on Monday and Tuesday evening and the other on Wednesday afternoon. The first, organized by Pallab Chatterjee and moderated by Steve Ohr, asks the question: "Is Quality a Design Constraint for Sub 100nm Designs?" The second evening panel on Tuesday night, organized by Marco Casale-Rossi, and moderated by A. Richard Goering, considers "The IC & Package Co-Design Challenge". Finally, the third panel organized by Giora Ben-Yaacov and moderated by Tets Maniwa looks at notion of "Hidden Quality, Crouching Customer - How much does the Quality of EDA Tools Impact Electronic Design?" Dinner will be served prior to the evening panel discussions. Come and hear the opinions of the leaders in the field, and voice your opinion during the audience participation phase for these controversial topics.

In summary, we have assembled an excellent program for academics, practicing engineers and managers in the IC industry to learn the latest on quality electronic design so that functional integrated circuits, with expected performance, acceptable yield and reliability, can be manufactured within the frame work of the desired cycle time. This conference provides a forum for you to learn, share and exchange insight and knowledge with your peers and to bridge the gap between the many functional areas that in total define the semiconductor IC industry. We welcome you to 2003.

Sincerely,

Ken Shepard
ISQED Technical Program Chair

Bharath Rajagopalan
ISQED Conference Chair

Vivek De
ISQED Technical Program Vice-Chair

Kaustav Banerjee
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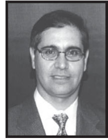

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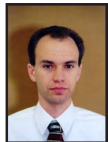

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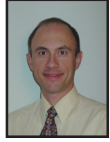

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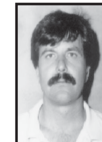

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ONFERENCE HIGHLIGHTS/GENERAL INFORMATION

ISQED 2003
GENERAL INFORMATION

March 24 - 26, 2003

DoubleTree Hotel
2050 Gateway Place
San Jose, CA
Telephone: 408-453-4000

TUTORIALS

Monday, March 24, 9:00 am - 4:45 pm
Features four parallel tracks with 14 tutorials. Includes lunch and coffee breaks.

PLENARY SESSIONS

Plenary Session I
Tuesday, March 25, 8:30 am - 10:15 am
Features keynote speeches by **Bob Payne** (US CTO & Senior Vice President/GM of System ASIC Technology Philips Semiconductors) **Susumu Kohyama** (Corporate Senior Vice President, Toshiba Corp.) and **Ted Vucurevich** (Senior Vice President & Chief Technical Office, Cadence Design Systems, Inc.)

Plenary Session II
Wednesday, March 26, 8:30 am - 10:15 am
Features keynote speeches by **Rajeev Madhavan** (Chairman & CEO, Magma Design Automation) **Michael Reinhardt** (President & CEO, RUBICAD Corp.) and **Shekhar Borkar** (Intel Corp.)

BEST PAPER AWARD

The ISQED 2003 Best Paper Award Ceremony will be held prior to the ISQED Plenary Presentations on Tuesday. The award will be presented to: **Paper# 6A-2, Design and Measurement of an Inductance-Oscillator for Analyzing Inductance Impact on On-Chip Interconnect Delay,** Takashi Sato, Hitachi, Ltd., Tokyo, Japan and Hiroo Masuda, Semiconductor Technology Academic Research Center Kanagawa, Japan. This paper will be presented on Wednesday, March 26, 4:05 pm in Session 6.

PANEL DISCUSSIONS

Evening Panel Discussion EP1 & Dinner
Monday, March 24, 6:30 pm - 8:30 pm

Is Quality a Design Constraint for Sub 100nm Designs?

Moderator:
Steven Ohr, EETimes

Evening Panel Discussion EP2 & Dinner
Tuesday, March 25, 6:30 pm - 8:30 pm

IC & Package Co-Design: Challenge or Dream?

Moderator:
Richard Goering, EETimes

Embedded Panel Discussion Session 5C
Wednessday, March 26, 1:00 pm - 3:05pm

Hidden Quality, Crouching Customer - How Much Does the Quality of EDA Tools Impact Electronic Design?

Moderator:
Tets Maniwa, Netronics Magazine

TECHNICAL SESSIONS

There are 16 technical sessions, featuring 39 papers accepted for oral presentation from 119 submitted to ISQED 2003. The program also includes 9 invited papers from leading experts in the field.

REGISTRATION INFORMATION

ADVANCE D REGISTRATION
For advanced registration, using the on-line registration process, visit the ISQED web site at www.isqed.org.

If you do not want to use the online registration process, complete the enclosed registration form and mail or fax it to the Symposium office.

ISQED Registrar
16220 South Frederick Avenue, Suite 312
Gaithersburg, MD 20877
Phone: 301-527-0900 x 101, Fax: 301-527-0994
Email: widerkehr@isqed.org

Do not register online and by mail or fax...it will result in duplicate billing.

Registrations must be received by March 14 to received the discounted rate. After March 14 you must register onsite at the Symposium.

Requests for cancellations must be received by March 19 in order to get a refund. Cancellations received after that date will not receive a refund. All refunds will be charged a $30 processing fee.

GENERAL INFORMATION

ON-SITE REGISTRATION
Due to limited space, you are encouraged to register in advance. On-site registration is available at the DoubleTree Hotel during registration hours.

ONSITE REGISTRATION DESK

The Registration Desk will be open as follows:

TUTORIAL REGISTRATION

Sunday, March 23	5:00 pm - 8:00 pm
Monday, March 24	8:00 am - 5:00 pm

TECHNICAL SESSION REGISTRATION

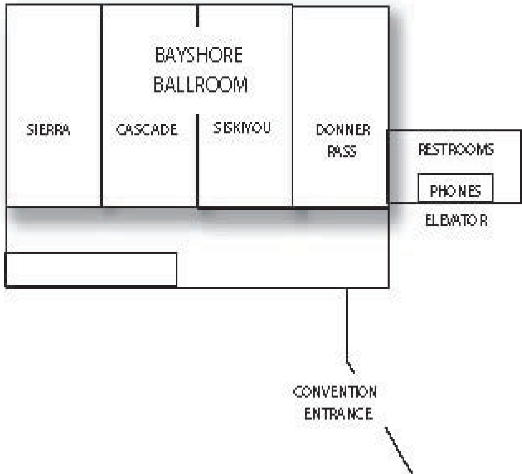
Monday, March 24	8:00 am - 5:00 pm
Tuesday, March 25	8:00 am - 5:00 pm
Wednessday, March 26	8:00 am - 3:00 pm

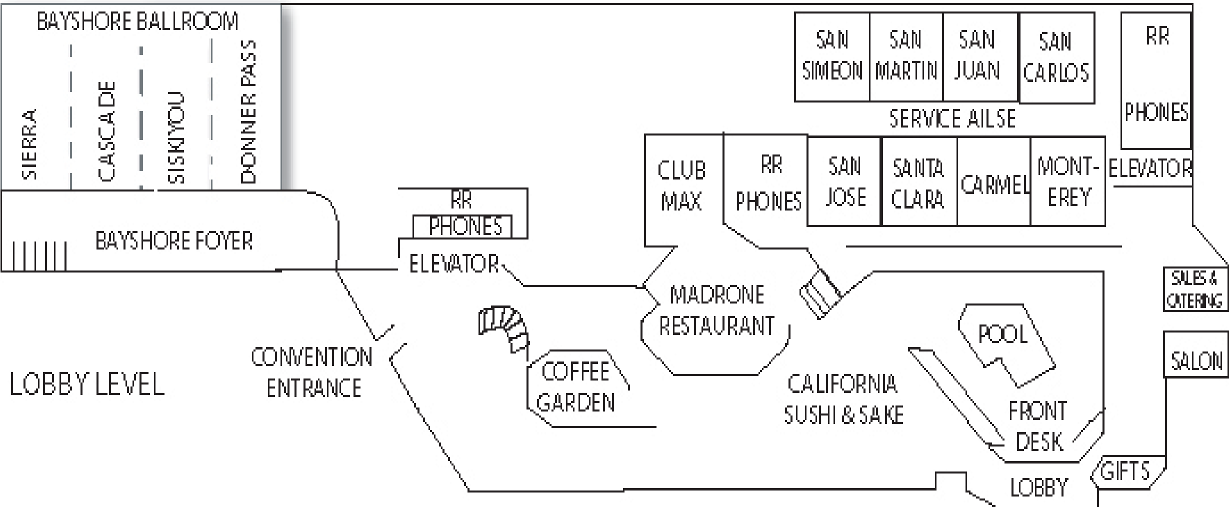
HOTEL RESERVATIONS

A block of rooms has been reserved at the DoubleTree Hotel for ISQED participants. The conference rate is $168 single/double plus 10.06% tax. There are two ways to make a reservation

1) through the ISQED website. Go to www.isqed.org, click on Register, scroll down and click on online reservations, scroll down and click on Book a Room.

2) or call the hotel at: 408-453-4000. Press 1 for reservations. If you call, be sure to tell reservations you are with the ISQED to qualify for the discounted room rate.





SYMPOSIUM AT A GLANCE

Date	Time	Room 1	Room 2	Room 3	Room 4
Monday 3/24/03	9:00 am - 4:45 pm	**Tutorial Track A** *Room: Monterey*	**Tutorial Track B** *Room: Carmel*	**Tutorial Track C** *Room: Santa Clara*	**Tutorial Track D** *Room: San Jose*
		Tutorials/Workshops Sponsored by Numerical Technologies			
	6:30 pm - 8:30 pm	**Evening Panel Discussion and Dinner** Is Quality a Design Constraint for Sub 100nm Designs? Sponsored by Ammocore *Room: Siskiyou*			
Tuesday 3/25/03	8:30 am - 10:15 am	**Plenary Session I** ISQED Best Paper Awards followed by Keynote Speeches by: Bob Payne, Susumu Kohyama, Ted Vucurevich *Room: Donner Pass*			
	10:15 am - 10:30 am	Break Sponsored by Magma			
	10:30 am - 12:00 pm	**Session 1A** Reliability and Design in Deep Submicron Technologies *Room: Monterey/Carmel*	**Session 1B** Reducing Leakage Currents in VLSI Circuits *Room: Santa Clara/San Jose*	**Session 1C** SoC Methodology *Room: San Carlos/San Juan*	
	12:00 pm - 1:00 pm	**ISQED Luncheon** Sponsored by Synopsys *Room: Siskiyou*			
	1:00 pm - 3:05 pm	**Session 2A** Testing of SoCs *Room: Monterey/Carmel*	**Session 2B** Design for Manu-facturability and Quality *Room: Santa Clara/San Jose*	**Session 2C** Design Considerations in Advanced Technologies *Room: San Carlos/San Juan*	
	3:05 pm - 3:30 pm	**Break** Sponsored by Magma			
	3:30 pm - 5:30 pm	**Session 3A** Interconnect and Substrate Noise *Room: Monterey/Carmel*	**Session 3B** Impact of New Standards for Design Data Modeling and Manufacturing Interface *Room: Santa Clara/San Jose*	**Session 3C** Package-Design Interface Challenges *Room: San Carlos/San Juan*	
	6:30 pm - 8:30 pm	**Evening Panel Discussion and Dinner** IC & Package Co-Design: Challenge or Dream? Sponsored by Advanced Packaging/PennWell *Room: Siskiyou*			
Wednesday 3/26/03	8:30 am - 10:15 am	**Plenary Session II** Keynote Speeches by: Rajeev Madhavan, Michael Reinhardt, Shekhar Borkar *Room: Donner Pass*			
	10:15 am - 10:30 am	Break Sponsored by Magma			
	10:30 am - 12:00 pm	**Session 4A** Power Analysis and Low Power Design *Room: Monterey/Carmel*	**Session 4B** Topics in Device and Interconnect Modeling *Room: Santa Clara/San Jose*	**Session 4C** Techniques for High-Speed Circuits and Module Generation *Room: San Carlos/San Juan*	
	12:00 pm - 1:00 pm	**Luncheon** *Room: Siskiyou*			
	1:00 pm - 3:05 pm	**Session 5A** Timing and Noise Issues in Physical Design *Room: Monterey/Carmel*	**Session 5B** Reliability Analysis *Room: Santa Clara/San Jose*	**Session 5C** Panel Discussion- Hidden Quality, Crouching Customer - How Much Does the Quality of EDA Tools Impact Electronic Design? Sponsored by Synopsys *Room: San Carlos/San Juan*	
	3:05 pm - 3:30 pm	**Break** Sponsored by Magma			
	3:30 pm - 5:30 pm	**Session 6A** Interconnect Parasitic Effects *Room: Monterey/Carmel*	**Session 6B** Design and Measurement Issues in Testing *Room: Santa Clara/San Jose*		

MONDAY TUTORIALS

Tutorial Track A
Design for Yield Optimization and Test
Monterey Room

Chair and Moderator: Yervant Zorian, Logic Vision

9:00am – 12:15pm

Tutorial A.1:

Integrating Yield, Test and Reliability: "Statistical Models with Applications to Test and Burn-in Optimization"

Organizer and Presenter: Adit Singh, Auburn University

Recent research has shown that die yield, test effectiveness, and early life reliability of integrated circuits are closely interrelated because of the common underlying statistics governing the distribution defects on semiconductor wafers. An understanding of these relationships can allow test effort, including burn-in screening, to be weighted in favor of sub population of dies with the highest expected failure rates. Consequently, the lowest possible defect levels (DPM) and field failure rates can be achieved at minimum overall test costs. This tutorial will introduce statistical yield-reliability models and show how they can be used for test optimization.

1:30pm – 4:45pm

Tutorial A.2:

Optimizing the Yield of VLSI Circuits

Organizer: Israel Koren, University of Massachusetts
Presenters: Julie Segal, HPL Technologies
Israel Koren, University of Massachusetts

Yield optimization effort must involve all area of semiconductor engineering: design, manufacturing, and test. This tutorial presents an overview of techniques for projecting and optimizing the yield of VLSI circuits, including high density memories, microprocessors and other architectures. Many of these techniques are being currently used in manufactured integrated circuits and will be reviewed. The nature of manufacturing defects is discussed in this tutorial, and the need for incorporating defect tolerance and/or yield enhancement techniques in the design of complex VLSI chips is explained. Then, some commonly used models for yield projection are presented. These models serve to evaluate the effectiveness of the proposed techniques and to calculate the optimal amount of circuit modifications.

Tutorial Track B
Design for Manufacutring and Yield
Carmel Room

Chair and Moderator: Duane Boning, MIT

9:00am – 10:30am

Tutorial B.1:

Testing and Yield of Integrated Circuits

Organizer and Presenter: Zoran Stamenkovic, IHP GmbH

Yield is one of the cornerstones of a successful integrated circuit (IC) manufacturing technology along with product performance and cost. Many factors contribute to the achievement of high yield but also interact with product performance and cost. A fundamental understanding of yield limitations enables the up-front achievement of this technology goal through circuit and layout design, device design, materials choices and process optimization. Defect, failure and yield analyses are critical issues for the improvement of IC yield. In first part, we deal with IC fault models and test issues. Second part describes critical area models and yield models. Third part is dedicated to a local extraction approach for the extraction of IC critical areas. Finally, we present an application of above-mentioned models and extraction approach in yield forecast.

10:45am – 12:15pm

Tutorial B.2:

Test Structures for Circuit Yield Assessment and Modeling

Organizer: Prof. Duane Boning , MIT
Presenters: Prof. Duane Boning , MIT
Prof. Anthony Walton, University of Edinburgh
Dr. Christopher Hess, PDF Solutions

The assessment and modeling of process variation and defectivity is becoming increasingly important in the design of high-yielding and high-performance integrated circuits. Process variation is coming from a number of sources: in addition to lot and wafer level variation, within chip variation arising from pattern dependencies is of substantial concern, affecting the matching of device and interconnect parameters. The understanding of defect sources and their impact and interaction with the layout continues to be critical to achieving required yields.

The focus of this tutorial session is on test structure methodologies for yield assessment and modeling. The first segment will describe a circuit-level test structure approach, which enables the extraction and characterization of layout practice and pattern dependent effects on delay in circuits. A scan-chain approach is coupled with a large number of ring oscillator variants, so that the impact of process and layout variations on realistic circuit timing can be extracted.

The second segment will describe test structures for measuring parametric characteristics such as linewidth, resistivity, contact resistance, layer thickness etc., as well as standard transistor parameters at the device level. Wafer mapping variations of these parameters with a view to identifying root causes will be briefly discussed. The section will conclude with the presentation of methods for increasing the number of devices on testchips through the use of active on-chip switching.

Finally, the third segment will describe "Universal Characterization Vehicles" that combine a variety of test structures on a single chip. It covers systematic and random yield characterization like defect densities, defect size distributions and fail rates, which are important input for DFM. It also includes structures that drive SPICE modeling including statistical SPICE models for advanced analog designs. Such vehicles can evaluate the entire process flow or just a fraction of it as a short loop to decrease cycle time. This segment will cover methods for advanced area usage as well as improved test procedures that significantly reduce test time.

1:30pm – 3:00pm

Tutorial B.3:

Design Based Yield Improvements (DBYI)

Organizer: Enrico Malavasi, PDF Solutions, Inc.
Presenters: Enrico Malavasi, PDF Solutions, Inc.
Stefano Tonello, PDF Solutions, Inc.

The manufacturability of integrated circuits can be improved at design level by incorporating modifications in the structure of the IP components (cores, cells, memories) and of interconnections, as well as changes in the design methodology and flow. In this tutorial we will describe the types of design improvements that can be introduced in the design of large integrated circuits, and the potential advantages they can have for yield. These include modifications in IP cores, standard cell libraries and memory blocks, as well as interconnections. The potential impact of different techniques on the design flow will also be discussed. We will describe the technology we use to quantitatively estimate and measure yield losses due to random, systematic and parametric effects. This capability is essential to drive design modifications, in order to understand their impact, and the trade-off between conflicting requirements.

3:15pm – 4:45pm

Tutorial B.4:

Yield in Flash Memory: Methodology, Modeling and Design Issues

Organizer and Presenter: Giuseppe Crisenza, STMicroelectronics

In the manufacturing of Flash Memory the main defective layers are metals, vias, polysilicon and contacts. Inside a Flash Memory, most of the area is utilized for memory array with around the decoding and multiplexing circuitry. In these regions, all buses in metal and polysilicon layers are designed with the minimum layout rules admitted by technology, to match the pitch dimension of the flash cells. As the number of steps, the number of cells, and the circuit density increases, and the critical defect sizes decreases, an increasing number of defects are only seen as electrical faults. Starting from the electrical signature to the physical defect identification, a collection of various defects, typical of Flash NOR array was identified and associated with methods for electrical screening. A yield model for Flash Memories with redundancy will show the effect of the three principal factors (systematic, defect and out layer related) allowing a faster analysis of yield limiting conditions. The decomposition of yield in the described factors allows the individuation of fields where the corrective actions have to be performed and the related strategies. For defectivity yield enhancement the corrective actions are the reduction of particles or point defects: in some case a simulation methodology is proposed in order to confirming the electrical signature. For systematic yield enhancement, robustness of the circuital blocks both layout and design , and of the testing flow are the principal issues addressed.

Tutorial Track C
IC and Package Co-Design

Santa Clara Room

Chair and moderator: Marco Casale-Rossi, ST Microelectronics

Driven by nanometer silicon process and system-on-chip (SOC) technologies, the complexity of today's integrated circuits (IC) combined with their high pin-count and performance requirements has resulted in a more complex silicon-package interface than seen with traditional devices.

To address these challenges companies are increasingly choosing ball-grid array (BGA) substrates and flip-chip as their preferred IC to package interconnect mechanism. While BGA offers a great deal of opportunities in terms of package customization, flip-chip addresses the high pin-count requirement and provides the benefit of reduced parasitics.

Unfortunately most design methodologies result in a segregated relationship between IC and package, making coordinated planning a difficult and time-consuming task. The serial nature of the traditional silicon to package design flow limits the effectiveness of existing tools for concurrent planning. Both IC and package design tools lack the needed visibility into their respective neighboring environments to be of use. This serial approach may lead to a poor IC to package netlist resulting in overly complex custom package designs, increased packaging costs, longer cycle times and less than optimal silicon performance. Although BGA and flip-chip provide a vehicle to interface high performance silicon to the system, a methodology change is needed to realize its full performance potential.

This tutorial will give an overview about BGA substrates—pointing-out the strengths and the limitations of flip-chip vs. wire-bonding, introduce the reasons and methods for co-design, and explore a new methodology that incorporates packaging as part of the silicon floor planning phase. New tools will be presented that facilitate coordinating planning and sharing of data across the two domains of silicon and package. The tutorial will show how coordinated planning during the early stages of IC floor planning will result in an optimized silicon/package interface, ultimately lowering cost, reducing cycle-time and enhancing overall device performance.

9:00am – 10:30am

Tutorial C.1:

A Package Design Perspective: "It Will Be BGA and Flip-Chip"

Presenter: Rich Evans, STMicroelectronics

1. BGA design flexibility
   a. BGA basics and configurations
   b. Pin-out and footprint
   c. Wire-bonding: signals, power, ground
   d. Flip-chip configurations
2. Discussion of the basic limitations of flip-chip
   a. Dimensions
   b. I/O count
   c. Limitations on design – bump size, pitch, reliability, substrate capability
   d. Examples
3. Reasons and methods for co-design
   a. Considerations for high I/O count, high performance design
   b. Reasons for flip-chip and for co-design
   c. Design variables
   d. System, IC, package requirements
   e. Examples of packages where co-design was applied
   f. Specific flip-chip design issues
4. Flip-chip electrical performance
   a. Inductance
   b. High-speed serial links
   c. Power distribution

10:45am – 12:15pm

Tutorial C.2:

An IC Design Perspective: "Why Would We Choose Flip Chip?"

Presenter: Scott Wood, STMicroelectronics

1. Design requirements that drive to flip-chip
   a. Large numbers of IO
   b. Large numbers of power/ground connections
   c. High performance packaging
   d. High power consumption
   e. Nominal die size
   f. Multiple power supplies
2. Tradeoffs in flip-chip
   a. Peripheral bumps vs. full array
   b. Peripheral IO vs. core array IO
3. CAD problems to be solved
   a. IO design
   b. IO placement
   c. single/multiple power grids
   d. Place and route
   e. Connectivity checking
   f. Co-design of PCB, substrate and silicon

1:30pm – 3:00pm

Tutorial C.3:

An EDA Perspective: "We Need It Yesterday!"

Presenter: Anna Fontanelli, STMicroelectronics

1. Today's design flows and their limitations
   a. Package driven, or top-down
   b. IC driven, or bottom-up
2. Co-design & co-verification
   a. Can do vs. worth doing, technology vs. economy
   b. Overlapping requirements
   c. IO and bumps placement
   d. Reliability
   e. Flip-chip
   f. Electrical & physical verification
3. Tools, methodologies and skills
   a. Current status @ ST
   b. Commercial vs. proprietary tools
   c. Interoperability issues
   d. Examples

3:15pm – 4:45pm

Tutorial C.4:

An EDA Perspective: "Let's Do It Concurrently!

Presenter: Kevin Rinebold, Synopsys

1. The silicon-package relationship
   a. Customers requests and industry responses
   b. Goals and challenges

2 Co-design
   a. Feasibility and trade-off analysis
   b. Concurrent IC & package design planning
   c. New tools and methodologies
   d. Examples

3 Co-verification
   a. Parasitic extraction and electrical modelling
   b. Full-chip characterization
   c. New tools and methodologies
   d. Examples

Tutorial Track D
Design for Reliability
San Jose Room

Chair and moderator: Mohsen Alavi, Intel Corporation

9:00am – 10:30am

Tutorial D.1:

Overview of Reliability Issues in Deep Sub-Micron Digital CMOS Technology and their Interaction with Circuit Design Considerations

Organizer and Presenter: Mohsen Alavi, Intel Corporation

During the operation of integrated circuits, electrical and thermal stress result in wear out of circuit components and degradation of key parameters and ultimately, catastrophic failure. Often times, failure of product functionality in meeting desired operating specifications occurs due to these parametric shifts and long before catastrophic failure. Therefore, circuits designed to allow larger shifts in parametric degradation result in enhanced product reliability. Such design practice requires good understanding of physical mechanisms resulting in degradation and good models to predict it's behavior vs. stress. Furthermore, understanding of the statistics of degradation is needed to evaluate overall product failure rates.

As technology scaling reduces device dimensions and increases circuit complexity, the challenge of ensuring product reliability increases in two ways. Namely, many degradation mechanisms such as electromigration or soft error become more pronounced while tools and techniques to model degradation in more complex circuits become more challenging. Moreover, the continuous pursuit of circuit performance often results in a trade off with reliability such as the case with higher Vcc for faster products vs. dielectric reliability.

This tutorial presents an overview of various physical mechanisms resulting in device degradation and their relation to stress conditions in MOS logic technology. For each degradation mechanism, circuit impact and design consequences will also be discussed. Mechanisms will include hot carrier effects, transistor bias-temperature stability, gate dielectric wear out, plasma induced gate charging, interconnect electromigration, electro-static discharge (ESD), and soft error. Future challenges posed by technology scaling will also be discussed.

10:30am – 12:15pm

Tutorial D.2:

Noise Analysis for 0.13µm and Beyond

Organizer: Ken Tseng, Cadence Design Systems
Presenters: Kishore Singhal, Agere Systems
Vinod (Narayanan) Kariat, Cadence Design Systems
Ken Tseng, Cadence Design Systems

At 0.13µm and beyond, ignoring signal integrity is a luxury no designer can afford; SI issues are no longer the purview of high-performance designs. Hence most designers need an awareness of Signal Integrity analysis, prevention and correction. The presenters will draw on their experiences in Signal Integrity over the last several years to present a pragmatic and practical tutorial on noise analysis, prevention and correction.

Section 1: Fundamental Principles
In this section, we will discuss the fundamental issues that give rise to noise in digital designs. This will start with the technology trends that are giving rise to an increase in noise problems. Then we cover different types of noise effects and the factors that govern them. We will also discuss the fundamental principles of noise analysis.

Section 2: Noise Analysis, Prevention and Correction
In this section, we will discuss how noise effects influence different stages of the design flow, from early prototyping to final layout, including prevention and correction techniques.

Section 3: Experience with Noise Issues in the Design Flow
In this section, we will discuss several practical considerations associated with putting noise analysis techniques into the design flow. We discuss the approaches that yield reasonable results in practice.

Section 4: Future Considerations
This section covers some of the emerging issues that we expect to surface in the future due to technological and manufacturing considerations. We will cover issues associated with Inductance, SOI, copper interconnect and various manufacturing rules.

1:30pm – 3:00pm

Tutorial D.3:

NBTI/HCI Modeling and Full-Chip Analysis in Design Environment

Organizer and Presenter: Lifeng Wu, Celestry

Hot-carrier (HC) degradation and negative bias temperature instability (NBTI) of MOS devices are the two most important reliability concerns for deep submicron (DSM) designs. HC degradation occurs when the channel electrons are accelerated in the high electric field near the drain of the MOS device and create interface states, electron traps, or hole traps in the gate oxide near the drain. LDD structure has become the standard drain structure to alleviate HC effects and the device-based DC criteria have been used extensively to qualify devices for HC reliability. It is becoming clear that these guidelines are too conservative for DSM technologies. It is therefore strongly desirable that circuit reliability simulation using a realistic AC (transient) circuit operation condition should be on the fingertips of the circuit designers to achieve the following goals: to maximize design performance by minimizing design guard-band, to speed up timing closure by reducing design iterations and to ensure circuit reliability by fixing design reliability problems. How to fit reliability simulation into the design environment is a more interesting topic from designer's perspective.

Compared to the more matured studies and solutions on HC effects, the studies on NBTI reliability has just started. NBTI reliability is becoming an increasingly important as the thickness of gate oxide film scaled down to less than 50 Angstrom, which is common for DSM designs. Unlike HC degradation which needs high electric field at the drain, NBTI effect can be significant even when the drain-source is zero biased. This implies that circuits could undergo NBTI stress even at standby operation condition! NBTI effect becomes more severe under high temperature stress. The popular burn-in procedure is being re-considered by designers to maintain acceptable yield. The recovery of NBTI effect is another important issue to reduce design margin.

This tutorial provides an overview of the HC and NBTI effects including physics, impact on circuit performance, modeling and simulation technologies. Both full-chip transistor-level and gate-level solutions will be presented with million-transistor/gate capacity and high accuracy.

Session EP1
Evening Panel Discussion & Dinner
Siskiyou Room

6:30pm - 8:30pm

Is Quality a Design Constraint for Sub 100nm Designs?

Organizer: Pallab Chatterjee, President and CEO
SiliconMap, LLC
Moderator: Steven Ohr, EETimes

Deep sub-micron design (below 100nm) present a number of new design challenges. These include very high masking costs, new interconnect materials and parasitic phenomenon, significant re-engineering at the device level due to changes in basic device performance, very high gate count and pin count designs, complexity in high pin count packaging & test, and finally reduced product life in the marketplace do to the rapid rollout of new technologies. One of the trade offs that is taking place in the industry to address these issues is the decision toward "design existence", which is the selection of the "first functional implementation" of a design, over "design quality" which is the selection of the "optimal implementation" of a design.

This panel will discuss the trends in the issue with respect to the re-targeting of the design quality issues from the SOC level to the flow and device levels and the impact on this "shift" on the manufacturability of the resulting designs. Issues discussed will include the use of pre-tested IP as a quality metric, the coverage and quality of the EDA design and validation tools, the correlation of these metrics to the actual manufacturing process and the impact of post fabrication process steps (packaging, test, etc.) on the yield of the resulting design.

Panelists:

Callen Carpenter
President and CEO
Silicon Metrics Corp.

Paul Kempf
CTO and VP Engineering
Jazz Semiconductor, Inc

John Kibarian
President and CEO
PDF Solutions, Inc.

Dennis Monticelli
Fellow at Natl Semiconductor, Inc.

Resve Saleh
NSERC/PMC Sierra Chair
Professor
UBC Vancouver

Norm Towson
President and CEO
Netcell Corporation

TUESDAY

Plenary Session I

Donner Room

8:30am - 10:15am

Co-Chairs: *Bharath Rajagopalan, ISQED Conference Chair*
Keneth Shepard, ISQED Technical Program Chair

8:30am

Welcome and Introduction
Best Paper Award Presentation

8:45am - 9:15am

1P.1 Platform Leadership in the Ambient Intelligence Era

Bob Payne, US CTO and Senior Vice President/GM of System ASIC Technology, Philips Semiconductors

Design reuse has become essential to cope with the ever-increasing design complexity. IP level reuse alone has proven insufficient. Platform based design allows the validation of a robust combination of IP blocks and provides a reference HW and SW baseline which can be supported with an integrated development environment. Several years ago we transitioned into the streaming data era with most systems serving as content generation appliances, content consumption appliances or content distribution equipment. Now we have entered the age of ambient intelligence where the streaming data is served up through wireless links. What will platform leadership look like in this new era? How will the SoC infrastructure change as we move to 90nm technology with more than 30M gate per square centimeter integration capacity? How are usage patterns changing and what represents the killer application that enhances the users quality of life by enabling more advanced interaction with the ambient intelligence? What is it going to take to make a step function improvement in system level design productivity? What happens when power optimization becomes the dominant design consideration? What about SoC affordability? What will the SoC design of the future look like? These are just some of the thought provoking issues that will be addressed in Bob Payne's keynote.

9:15am - 9:45am

1P.2 Quality SoC Design and Implementation for Real Manufacturability

Susumu Kohyama, Corporate Senior Vice President, Toshiba Corporation

Device miniaturization near 100nm node and beyond together with extreme multi-level interconnect started to create fundamental economical and engineering challenges. Especially, past success model of "Layer Masters" confessed difficulties to fill the gaps between each separated layers to complete integrated results, for meeting performance and yield with a reasonable timing. However, it is also obvious that classic IDM model proved to be so inefficient, since inevitable separation and standardization of various aspects of design and technology are not established adequately. Those issues are even more significant when we discuss complex SoCs for 90nm and 65nm nodes, where design and implementation commingle in various different manners. A solution for these challenges is a new open IDM model where open collaboration and strong differentiator are essential.

This presentation will discuss from a "SoC centric Open IDM" perspective, the whole flow of design and implementation for real manufacturability, where true knowledge of integration and management skill function to enhance differentiators on top of open platforms.

9:45am - 10:15am

1P.3 Quality Challenges of the Nanometer Design Realm

Ted Vucurevich, Senior Vice President and Chief Technical Office, Cadence Design Systems, Inc.

It is commonly agreed that sub-nanometer design is electronic design technology's next big challenge. With the economic stakes higher than ever, the vendors of electronic design solutions must put themselves into their customers' shoes through comprehensive, high-quality programs. My understanding of the differences designers face at geometries below 100 nanometers has led to my discussion of some of the challenges the industry faces in the sub-nanometer realm. This includes the domination of wires in digital design, which requires the ability to design the best quality wires through continuous convergence, a wire-centric methodology. In the nanometer world, the front-end and back-end disappear, leaving the prototype as the chip. This includes detailed wiring, and a new full-chip iteration every day. Most sub-nanometer ICs and SoCs will be digital/mixed-signal. This leads to custom design issues, such as integrating sensitive circuits with massive digital and mixed-signal design, productivity and foundry interface. Nanometer SoC verification includes digital, analog and software, and a 70 percent silicon re-spin rate because of associated functional errors. At sub-nanometer levels, design-in becomes a major bottleneck, especially across a design chain, which can only be solved by silicon-package-board co-design.

TUESDAY

Session 1A

Monterey/Carmel Room

10:30am - 12:00pm

Reliability and Design in Deep Submicron Technologies

Co-Chairs: Ajith Amerasekera, Texas Instruments

10:30am
Introduction

10:35am
1A-1 Reliability Evaluation for Integrated Circuit with Defective Interconnect under Electromigration, Xiangdong Xuan, Adit Singh[1], Abhijit Chatterjee, Georgia Institute of Technology, Atlanta, GA and [1]Auburn University, Auburn, AL

11:05am
1A-2 Analysis of IR-Drop Scaling with Implications for Deep Submicron P/G Network Designs, Amir Ajami, Kaustav Banerjee[1], Massoud Pedram[2], Amit Mehrotra[3], Magma Design Automation, Cupertino, CA, [1]University of California at Santa Barbara, CA, [2]University of Southern California and [3]University of Illinois at Urbana-Champaign, Urbana, IL

11:35am
1A-3 Random Sampling for On-Chip Characterization of Standard-Cell Propagation Delay, Stefano Maggioni, Andrea Veggetti, Alessandro Bogliolo[1], Luigi Croce, STMicroelectronics, Agrate, Italy and [1]University of Urbino, Urbino, Italy

Session 1B

Santa Clara/San Jose Room

10:30am - 12:00pm

Reducing Leakage Currents in VLSI Circuits

Co-Chairs: Payam Heydari, University of California, Irvine
Khorram Muhammad, Texas Instruments

10:30am
Introduction

10:35am
1B-1 Leakage Current Reduction in Sequential Circuits by Modifying the Scan Chains, Afshin Abdollahi, Farzan Fallah[1], Massoud Pedram, University of Southern California, Los Angeles, CA and [1]Fujitsu Laboratories of America, Sunnyvale, CA

11:05am
1B-2 Comparative Assessment of Adaptive Body-Bias SOI Pass-Transistor Logic, Geun Rae Cho and Tom Chen[1], Colorado State University, Fort Collins, CO and [1]Hewlett Packard, Fort Collins, CO

11:35am
1B-3 Design Techniques for Gate-Leakage Reduction in CMOS Circuits, Rafik Guindi, Farid Najm, University of Toronto, Toronto, Ont., Canada

Session 1C

San Carlos/San Juan Room

10:30am - 12:00pm

SoC Methodology

Co-Chairs: Vamsi Srikantam, Agilent Technologies
Tom Chen, Colorado State University

10:30am
Introduction

10:35am
1C-1 Using Integer Equations for High Level Formal Verificaiton Property Checking, Bijan Alizadeh, Mohammad Kakoee, University of Tehran, Tehran, Iran

11:05am
1C-2 True Coverage: A Goal of Verification, Gary Feierbach, Vijay Gupta, Apple Computer, Cupertino, CA

11:20am
1C-3 Real-Time and Low-Cost Incremental Super-Resolution Over a Video Encoder IP Block, Gustavo Marrero Callico, Rafael Peset Llopis[1], Antonio Nunez, Ramanathan Sethuraman[1], University of Las Palmas de Gran Canaria, Canary Islands, Spain and [1]Philips Research Laboratories, Eindhoven, The Netherlands

11:35am
1C-4 LYS: A Solution for System on Chip (SoC) Produciton Cost and Time to Volume Reduction, Jean-Pierre Heliot, Florent Parmentier, Marie-Pierre Baron, STMicroelectronics, Crolles, France

Session 2A

Monterey/Carmel Room

1:00pm - 3:05pm

Testing of SoCs

Co-Chairs: Sreejet Chakravarty, Intel Corporation
Jacob Abraham, University of Texas

1:00pm
Introduction

1:05pm
2A-1 Solving the SoC Test Scheduling Problem Using Network Flow and Reconfigurable Wrappers, Sandeep Koranne, Tanner Research Inc., Pasadena, CA

1:35pm
2A-2 Static Pin Mapping and SOC Test Scheduling for CORES with Multiple Test Sets, Yu Huang, Wu-Tung Cheng, Chien-Chung Tsai, Nilanjan Mukherjee, Sudhakar Reddy[1], Mentor Graphics Corp., Waltham, MA and Wilsonville, OR, [1]University of Iowa, Iowa City, IA

2:05pm
2A-3 Compact Dictionaries for Fault Diagnosis in BIST, Chunsheng Liu, Krishnendu Chakrabarty, Duke University, Durham, NC

2:35pm
2A-4 Automated Synthesis of Configurable Two-Dimensional Linear Feedback Shifter Registers for Random/ Embedded Test Patterns, Chien-In Henry Chen, Wright State University, Dayton, OH

Session 2B

Santa Clara/San Jose Room

1:00pm - 3:05pm

Design for Manufacturability and Quality

Co-Chairs: Sharad Saxena, PDF Solutions
Jay Michlin, Consultant

1:00pm
Introduction

1:05pm
2B-1 Design and Use of Memory-Specific Test Structures to Ensure SRAM Yield and Manufacturability, F. Duan, R. Castagnetti, R. Venkatraman, O. Kobozeva, S. Ramesh, LSI Logic Corp., Milpitas, CA

1:35pm
2B-2 Advanced Physical Models for Mask Data Verification and Impacts on Physical Layout Synthesis, Qi-De Qian, Sheldon Tan[1], IC Scope Research, Santa Clara, CA, [1]University of California, Riverside, CA

2:05pm
2B-3 New DFM Approach Abstracts AltPSM Lithography Requirements for Sub-100nm IC Design Domains, Pradiptya Ghosh, Chung-shin Kang, Michael Sanie, David Pinto, Numerical Technologies, San Jose, CA

2:35pm
2B-4 Methods and Framework for QA of Process Design Kits, Matthew Scott, Michael Peralta, J.D. Carothers[1], Paul Koch, Texas Instruments, Tucson, AZ, [1]University of Arizona, Tucson, AZ

2:50pm
2B-5 The iFlow Design Factory: Evolving Chip Design from an Art to a Process, through Adaptive Resource Management, and Qualified Data Exchange, Gilles-Eric Descamps, Satish Bagalkotkar, Subramanian Ganesan, Sridhar Subramaniam, Hem Hingarh, Silicon Access Networks, San Jose, CA

Session 2C

San Carlos/San Juan Room

1:00pm - 3:05pm

Design Considerations in Advanced Technologies

Co-Chairs: Ken Shepard, Columbia University
Vivek De, Intel Corporation

1:00pm
Introduction

1:05pm
2C-1 Design Considerations of Scaled Sub-0.1µm PD/SOI CMOS Circuits (Invited), Ching-Te (Kent) Chuang, IBM

1:35pm
2C-2 Revisiting the Noise Figure Design Metric for Digital Communication Receivers (Invited), Won Namgoong, University of Southern California

2:05pm
2C-3 Bechnmarks for Interconnect Parasitic Resistance and Capacitance (Invited), N.S. Nagaraj, Texas Instruments

Session 3A

Monterey/Carmel Room

3:30pm - 5:30pm

Interconnect and Substrate Noise

Co-Chairs: Sarma Vrudhula, University of Arizona
Amit Majumdar, Sun Microsystems

3:30pm
Introduction

3:35pm
3A-1 Post-Route Gate Sizing for Crosstalk Noise Reduction, Murat Becer, David Blaauw[1], Ilan Algor[2], Rajendran Panda, Chanhee Oh, Vladimir Zolotov, Ibrahim Hajj[3], Motorola Inc., Austin, TX, [1]University of Michigan, Ann Arbor, MI and [2]Motorola Semiconductor Israel Ltd., Israel, [4]University of Illinois, Urbana, IL

4:05pm
3A-2 Noise Aware Driver Modeling for Nanometer Technology, Xiaoliang Bai, Rajit Chandra[1], Sujit Dey, Prasanna Srinivas[1], University of California, San Diego, La Jolla, CA and [1]Magma Design Automation, Cupertino, CA

4:35pm
3A-3 Analyzing Statistical Timing Behavior of Coupled Interconnects Using Quadratic Delay Change Characteristics, Tom Chen, Amjad Hajjar[1], Hewlett Packard, Fort Collins, CO and [1]Colorado State University, Fort Collins, CO

4:50pm
3A-4 Modeling Crosstalk Induced Delay, Chung-Kuan Tsai, Malgorzata Marek-Sadowska, University of California, Santa Barbara, CA

5:05pm
3A-5 A CAD-Oriented Modeling Approach to Frequency-Dependent Behavior of Substrate Noise Coupling for Mixed-Signal IC Design, Hai Lan, Zhiping Yu, Robert Dutton, Stanford University, Stanford, CA

Session 3B

Santa Clara/San Jose Room

3:30pm - 5:30pm

Impact of New Standards for Design Data Modeling and Manufacturing Interface

Co-Chairs: Andrew Kahng, University of California, San Diego
Tom Chen, Colorado State University

3:30pm
Introduction

3:35pm
3B-1 Assessment of the OpenAccess Standard: Insights on the New EDA Industry Standard From Hewlett Packard, an Early Beta Partner and Contributing Development (Invited), Terry Blanchard, Hewlett Packard

4:05pm
3B-2 Impact of Interoperability on CAD-IP Reuse (Invited), Igor Markov, University of Michigan

4:35pm
3B-3 Interoperability Beyond Design: Sharing Knowledge Between Design and Manufacturing (Invited), Don Cottrell, Si2

Session 3C

San Carlos/San Juan Room

3:30pm - 5:30pm

Package-Design Interface Challenges

Co-Chairs: Ali Iranmanesh, Celeritek
Ken Shepard, Columbia University

3:30pm
Introduction

3:35pm
3C-1 Advanced Module Packaging Method, Peter Salmon, SysFlex, Sunnyvale, CA

4:05pm
3C-2 Electrical and Thermal Analysis for System-in-a-Package (SiP) Implementation Platform, Michael Wang, Katsuharu Suzuki, Wayne Dai, University of California, Santa Cruz, CA

4:35pm
3C-3 Modeling and Analysis of Power Distribution Networks for Gigabit Applications, Wendem Beyene, Chuck Yuan, Joong-Ho Kim[1], Madhavan Swaminathan[1], Rambus, Inc. Los Altos, CA and [1]Georgia Institute of Technology, Atlanta, GA

5:05pm
3C-4 Active Device Under Bond Pad to Save I/O Layout for High-Pin-Count SOC, Ming-Dou Ker, Jeng-Jie Peng[1], Hsin-Chin Jiang[1], National Chiao-Tung University, Taiwan and [1]ITRI, Taiwan

Session EP2
Evening Panel Discussion & Dinner

Siskiyou Room

6:30pm -8:30pm

IC & Package Co-Design: Challenge or Dream?

Organizer: Marco Casale-Rossi, STMicroelectronics
Moderator: Richard Goering, EETimes

In recent years, major breakthroughs have occurred in packaging technology, which have led to the industrialization of several kinds of new packages, more powerful, and yet more flexible, in the attempt to cope with the challenges posed by multi-million gates and multi-GHz systems-on-a-chip (SOC). While offering a great deal of opportunities, ball-grid array (BGA) substrates, flip-chip and multi-stacked dies require an unprecedented level of integration between IC and package design and verification.

This integration, however, requires a change in methodology, with the availability of new EDA tools, and a major shift in the profile of the designers and engineers involved which, to a certain extent, have to acquire each other competences.

Although necessary, this cannot be given for granted. While BGA is a reality, flip-chip is still a question mark for the majority of the applications, due to both cost reasons and lack of commercial EDA tools. A package re-use discipline is becoming a must to avoid a package design start for each IC design start, with expensive substrates scraps. How to implement it? Interoperability between Cadence and Synopsys and the rest of the EDA world is a key aspect, as customers don't want to be further bound to few vendors—nor wants the FTC! How to enforce it?

This panel is not about packages nor about ICs, it's about whether today's electronic systems can be successfully designed and assembled in their target package, without taking into consideration each other requirements since the very early beginning. It's about the requirements, the challenges and the on-going initiatives, if any.

Panelisits:

Dr. Raul Camposano
CTO, Synopsys

Carlo Cognetti
VP Corp. Package Dev.
STMicroelectronics

Nitin Deo
VP Business Development
Magma Design Automation

Aurangzeb Khan
VP Design Foundry
Cadence Design Systems

Dr. Lou Scheffer
Architect
Cadence Design Systems

Plenary Session II
Donner Room

8:30am - 10:15am

Co-Chairs: Kaustav Banerjee, ISQED Conference Vice Chair
Kris Verma, ISQED Plenary Chair

8:30am
Welcome and Introduction

8:45am - 9:15am
2P.1 Addressing the IC Designer's Needs: Integrated Design Software for Faster,More Economical Chip Design

Rajeev Madhavan, Chairman & CEO, Magma Design Automation

Electronic design automation continues to attract a great deal of investment from the venture community, fostering the creation of startup companies focused on developing unique point-tool solutions. While many innovative new technologies come from this, industry must consider the increasingly critical need of IC designers and manufacturers: integrated design flows that enable the design and production of chips with fewer resources and in less time, without compromising the quality of results. Increasingly evident is the advantage of integrated design and the economies it brings while delivering the same quality of results as point-tool-based approaches. The future of EDA depends on the industry's ability to deliver solutions that enable the IC industry's integration of electronic design tools and processes as it relies on EDA to provide the means for producing the next generation of semiconductor products.

9:15am - 9:45am
2P.2 Closing the Gap between ASIC and Full Custom: A Path to Quality Design

Michael Reinhardt, President & CEO, RUBICAD Corporation

Although process technology has shrunk down to nanometer features over the last decade, the gap between ASIC design and full-custom IC design has widened. This gap includes significant differences in performance, price, and profit between the two design styles. It is also revealed by huge differences in quality between the two styles in speed, power distribution and consumption, yield, and reliability, in some cases as much as an order of magnitude. To fully utilize the latest process technologies, a full-custom design approach with the productivity of an ASIC flow is necessary.
Michael Reinhardt will start with an analysis of how the gap between ASIC and full-custom design began, and discuss its long-term consequences on the whole industry. He will then show the positive effects on the quality of IC design, and on the chip industry's economic situation, which can occur if this gap can be closed. He will illustrate possible strategies and solutions for achieving this closure, and how they can be implemented right now in practical ways.

9:45am - 10:15am
2P.3 A VLSI System Perspective for Microprocessors Beyond 90nm

Shekhar Borkar, Fellow & Director of Circuit Research Lab, Intel Corporation

Microprocessor performance increased by five orders of magnitude in the last three decades. This was made possible by continued technology scaling, improving transistor performance to increase frequency, increasing integration capacity to realize complex architectures, and reducing energy consumed per logic operation to keep power dissipation within limit. The technology treadmill will continue to fulfill the microprocessor performance demand; however, with some adverse effects posing barriers—limited by power delivery and dissipation—and not by manufacturing or cost. Therefore, performance at any cost will not be an option; significant improvements in efficiency of transistor utilization will be necessary. This talk will discuss potential solutions in all disciplines, such as microarchitecture, circuits, design technologies & methodologies, thermals, and power delivery, to overcome these barriers for microprocessors beyond 90nm.

WEDNESDAY

Session 4A

Monterey/Carmel Room

10:30am - 12:00pm

Power Analysis and Low Power Design

Co-Chairs: Rajiv Joshi, IBM
Alireza Keshavarzi, Intel Corporation

10:30am
Introduction

10:35am
4A-1 Optimizing the Energy-Delay-Ringing Product in On-Chip CMOS Line Drivers, Soroush Abbaspour, Massoud Pedram, Payam Heydari[1], University of Southern California, Los Angeles, CA and [1]University of California-Irvine, Irvine, CA

11:05am
4A-2 Cycle-Accurate Energy Measurement and High-Level Measurement and High-Level Energy Characterization of FPGAs, Hyung Gyu Lee, Sung Yuep Nam, Naehyuck Chang, Seoul National University, Seoul, Korea

11:35am
4A-3 Quantifying Error in Dynamic Power Estimation of CMOS Circuits, Puneet Gupta, Andrew Kahng, University of California at San Diego, La Jolla, CA

11:50am
4A-4 Monolithic DC-DC Converter Analysis and MOSFET Gate Voltage Optimization, Volkan Kursun, Siva Narendra1, Vivek De[1], Eby Friedman, University of Rochester, Rochester, NY and [1]Intel Corp., Hillsboro, OR

Session 4B

Santa Clara/San Jose Room

10:30am - 12:00pm

Topics in Device and Interconnect Modeling

Co-Chairs: Janet Wang, Cadence Design Systems
Amit Mehrotra, University of Illinois, Urbana

10:30am
Introduction

10:35am
4B-1 Analysis of Simultaneous Subthreshold and Gate-Oxide Tuneling Leakage Current in Nanometer CMOS Design, Wesley Kwong, Dongwoo Lee, David Blaauw, Dennis Sylvester, University of Michigan, Ann Arbor, MI

11:05am
4B-2 Design and Analysis of Low-Voltage Current-Mode Logic Buffers, Peyam Heydari, University of California, Irvine, CA

11:35am
4B-3 Reduced-Order Modeling Based on PRONY's and SHANK's Methods via the Bilinear Transformation, Makram Mansour, Amit Mehrotra, University of Illinois at Urbana-Champaign, Urbana, IL

Session 4C

San Carlos/San Juan Room

10:30am - 12:00pm

Techniques for High Speed Circuits and Module Generation

Co-Chairs: James Lei, Altera Corporation
Andrew Kahng, University of California, San Diego

10:30am
Introduction

10:35am
4C-1 Parameterized Macrocells with Accurate Delay Models for Core-Based Designs, Makram Mansour, Mohammad Mansour, Amit Mehrotra, University of Illinois at Urbana-Champaign, Urbana, IL

11:05am
4C-2 Procedural Analog Design (PAD) Tool, Danica Stefanovic, Maher Kayal, Marc Pastre, Vanco Litovski[1], Swiss Federal Institute of Technology, Lausanne, Switzerland and [1]University of Nis, Nis, Yugoslavia

11:35am
4C-3 A Novel Clocking Strategy for Dynamic Circuits, Young Jun Lee, Yong-Bin Kim, Northeastern University, Boston, MA

Session 5A

Monterey/Carmel Room

1:00pm - 3:05pm

Timing and Noise Issues in Physical Design

Co-Chairs: Tanay Karnik, Intel Corporation
Rajiv Murgaii, Fujitsu

1:00pm
Introduction

1:05pm
5A-1 Clock Scheduling for Power Supply Noise Suppression Using Genetic Algorithm with Selective Gene Therapy, Wai-Ching Douglas Lam, Cheng-Kok Koh, Purdue University, West Lafayette, IN

1:35pm
5A-2 Minimizing Inter-Clock Coupling Jitter, Ming-Fu Hsiao, Malgorzata Marek-Sadowska[1], National Taiwan University,

Fremont, CA and [1]University of California, Santa Barbara, CA

2:05pm
5A-3 A Proposal for Routing-Based Timing-Driven Scan Chain Ordering, Puneet Gupta, Stefanus Mantik[1], Andrew Kahng, University of California at San Diego, La Jolla, CA and [1]Cadence Design Systems, Inc., San Jose, CA

2:20pm
5A-4 A False Agressor Elimination Method Using Functional Relationship for Full-Chip Crosstalk Analysis, Jae-Seok Yang, Jeong-Yeol Kim, Joon-Ho Choi, Moon-Hyun Yoo, Jeong-Taek Kong, Samsung Electronics Co., Ltd., Gyeonggi-do, Korea

2:35pm
5A-5 PDL: A New Physical Synthesis Methodology (Invited), Toshiyuki Shibuya, Rajeev Murgai[1], Tadashi Konno, Kazuhiro Emi, Kaoru Kawamura, Fujitsu Labs, Kawasaki, Japan, [1]Fujitsu Labs of America, Sunnyvale, CA

Session 5B

Santa Clara/San Jose Room

1:00pm - 3:05pm

Reliability Analysis

Co-Chairs: Jayasimha Prasad, Micrel Semiconductor
Olof Tornblad, Infineon

1:00pm
Introduction

1:05pm
5B-1 Statistical Modeling for Circuit Simulation (Invited), Colin McAndrew, Motorola, Tempe, AZ

1:35pm
5B-2 Electrostatic Discharge Implantation to Improve Machine-Model ESD Robustness of Stacked NMOS in Mixed-Voltage I/O Interface Circuits, Ming-Dou Ker, Hsin-Chyh Hsu, Jeng-Jie Peng[1], National Chiao-Tung University, Taiwan and [1]Industrial Technology Research Institute, Taiwan

2:05pm
5B-3 Coupled Simulation of Circuit and Piezoelectric Laminates, Chenggang Xu, Terri Fiez, Kartkeya Mayaram, Oregon State University, Corvallis, OR

2:20pm
5B-4 Investigation of the Capacitance Deviation Due to Metal-Fills and the Effective Interconnect Geometry Modeling, Won-Seok Lee, Keun-Ho Lee, Jin-Kyu Park, Tae-Kyung Kim, Young-Kwan Park, Jeong-Taek Kong, Samsung Electronics Co., Ltd., Kyunggi-do, Korea

2:35pm
5B-5 Static Electromigration Analysis for Signal Interconnects, David Blaauw, Vladimir Zolotov[1], Chanhee Oh[1], Murat Becer[1], Rajendran Panda[1], University of Michigan, Ann Arbor, MI and [1]Motorola, Inc., Austin, TX

Session 5C

San Carlos/ San Juan Room

1:00pm - 3:05pm

Afternoon Panel: Hidden Quality, Crouching Customer - How Much Does the Quality of EDA Tools Impact Electronic Design?

Organizer: Giora Ben-Yaacov, Quality Architect, Synopsys
Moderator: Tets Maniwa, Editor in Chief, Netronics Magazine

In today's fast-paced electronics market, design engineers face incredible challenges keeping up with increasingly complex technology and time-to-market pressures. Many design engineers facing these challenges say that quality problems with their EDA tools cost them dearly in lost productivity and in missed deadlines. At the same time, the same design engineers also say that they urgently need better technology, features, and special functions in the EDA tools they use in their work.

Thus, quality in EDA products is crucial to customer success - or is it? How much quality is enough to keep the industry moving at its fast pace? Is quality a hidden dragon that could cause customers to crouch in fear? What are the costs and who will pay for higher quality? Can EDA customers have their cake and eat it too?

Examples of some provocative questions that can be posed are:

"For the user - is EDA quality worth the hype at the expense of technology?"

"Do mainstream and power users want higher quality or more functionality"

"Do users of front-end and back-end tools require different level of quality?"

This panel will examine the core issues of quality in EDA products and the impact on electronic design — from the viewpoints of customers, EDA vendors and independent analysts.

Panelists:

Rahul Goyal
Director, EDA Business and Technology Programs
Intel Corporation

Scott Sandler,
President and CEO
Novas Software

Rich Goldman
Vice President, SVP
Quality and Interoperability
Synopsys, Inc.

Gary Smith
EDA Director and Chief Analyst
Dataquest

Rob Mains
Senior Design Automation Architect
Sun Microsystems

WEDNESDAY

Session 6A

Monterey/ Carmel Room

3:30pm - 5:30pm

Interconnect Parasitic Effects

Co-Chairs: *Dennis Sylvester, University of Michigan*
Rajendran Panda, Motorola

3:30pm
Introduction

3:35pm
6A-1 On-Chip Interconnect Inductance - Friend or Foe (Invited), Simon Wong, Stanford University, Stanford, CA

4:05pm
6A-2 Design and Measurement of an Inductance-Oscillator for Analyzing Inductance Impact, Takashi Sato, Hiroo Masuda[1], Hitachi, Ltd., Tokyo, Japan and [1]Semiconductor Technology Academic Research Center, Kanagawa, Japan

4:35pm
6A-3 On the Accuracy of Return Path Assumption for Loop Inductance Extraction for 0.1µm Technology and Beyond, SoYoung Kim, Yehia Massoud[1], S. Simon Wong, Stanford University, Stanford, CA and [1]Synopsys Inc., Mountain View, CA

4:50pm
6A-4 Impact of Interconnect Pattern Density Information on a 90nm Technology ASIC Design Flow, Payman Zarkesh-Ha, S. Lakshminarayann, Ken Doniger, William Loh, Peter Wright, LSI Logic Corp., Milpitas, CA

5:05pm
6A-5 Analyzing the Internal-Switching Induced Simultaneous Switching Noise, Li Yang, J.S. Yuan, M. Hagedorn[1], University of Central Florida, Orlando, FL, [1]Theseus Logic, Inc., Maitland, FL

Session 6B

Santa Clara/ San Jose Room

3:30pm - 5:30pm

Design and Measurement Issues in Testing

Co-Chairs: *George Alexioux, University of Patras*
Daneila De Venuto, Polytechnic of Bari

3:30pm
Introduction

3:35pm
6B-1 Generation of Combinational Hazard Identification Functions, Maria Michael, Spyros Tragoudas[1], University of Notre Dame, Notre Dame, IN and [1]Southern Illinois University, Carbondale, IL

4:05pm
6B-2 Concurrent Fault Detection in Random Combinational Logic, Petros Drineas, Yiorgos Makris, Yale University, New Haven,CT

4:35pm
6B-3 Automatic Repositioning Technique for Digital Cell Based Window Comparators and Implementation within Mixed-Signal DFT Schemes, Daniela De Venuto, Michael Ohletz[1], Bruno Ricco[2], Politecnico di Bari, Bari, Italy, [1]AMI Semiconductor Belgium, Zaventem, Belgium and [2]University di Bologna, Bologna, Italy

5:05pm
6B-4 On Structural vs. Functional Testing for Delay Faults, Angela Krstic, Jing-Jia Liou[1], Tim Cheng, Li-C. Wang, University of California, Santa Barbara, CA and [1]National Tsing Hua University, Hsinchu, Taiwan

5:20pm
6B-5 An Embedded Iddq Testing Architecture and Technique, Y. Tsiatoushas, Th. Haniotakis[1], A. Arapoyanni[2], University of Ioannina, Ioannina, Greece, [1]Southern Illinois University, Carbondale, IL, [2]University of Athens, Athens, Greece