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Call for Papers

ISQED China 2014
16th International Symposium & Exhibits on

QUALITY ELECTRONIC DESIGN

Oct. 27-29 2014. Hangzhou, China

Paper Submission Deadline: April 25 2014
Acceptance Notifications: July 1, 2014
Final Camera-Ready paper: Aug. 1, 2014

A pioneer and leading interdisciplinary electronic design and semiconductor conference, ISQED accepts and promotes papers in following areas:

- ***Sensors Technology, Design and Applications, MEMS/NEMS***
- ***Mobile Internet and Internet of Things: Technology, Design and Applications***
- ***Antennas Technology, Design and Applications, Wireless Power Transfer***
- ***System-level Design, Methodologies & Tools***
- ***FPGA Architecture, Design, and CAD***
- ***Design of Embedded Systems***
- ***Advanced 3D ICs & 3D Packaging, and Co-Design***
- ***Robust & Power-conscious Circuits & Systems***
- ***Emerging/Innovative Device Technologies and Design Issues***
- ***Design of Reliable Circuits and Systems***
- ***IP Design, quality, interoperability and reuse***
- ***Design Verification and Design for Testability***
- ***Physical Design, Methodologies & Tools***
- ***EDA Methodologies, Tools, Flows***
- ***Design for Manufacturability/Yield & Quality***
- ***Effects of Technology on IC Design, Performance, Reliability, and Yield***

Papers from past ISQED events have been published in ISQED proceedings and IEEE Xplore.

For more information please visit:

www.ISQED.org/China

WELCOME TO ISQED 2014

On behalf of the ISQED 2014 conference and technical committees, we are pleased to welcome you to the 15th International Symposium on Quality Electronic Design, ISQED 2014. This conference is the premier multidisciplinary design and design automation conference, aimed at bridging the gap between and integration of, electronic design tools and processes, integrated circuit technologies, processes, and manufacturing, to achieve design quality.

ISQED continues to provide and foster a unique opportunity to participants to interact and engage themselves in cutting edge tutorials, presentations, and panel and plenary sessions. We are happy to report a number of initiatives this year. The conference is organized around the theme 'Security in a Connected World.' We have invited several distinguished keynote speakers from both industry and academia to discuss breakthroughs and future trends in a new era of computing, hardware-software co-design, Internet-of-Things, and Cloud-delivered services with a focus on security related topics.

ISQED tutorials provide a holistic approach, from devices to circuits to systems, while covering in-depth studies and state-of-the-art in each of the topics impacting the quality of electronic design. The two-day technical program with three parallel sessions pack over 100 papers highlighting the latest trends in electronic circuit and system design & automation, test, verifications, and semiconductor technologies.

We are happy to report a 14% increase in the number of papers submitted this year. A new track on Smart Sensors Design Technology is formed to bring forth the technical innovations and trends in electronic design in this ever growing and ubiquitous field.

All the technical presentations, plenary sessions, tutorials and related events will take place on March 3-5 at the Santa Clara Convention Center in Santa Clara, CA. Please refer to the conference booklet and/or ISQED website for program details.

We would like to thank the ISQED 2014 corporate sponsors: IBM, Synopsys, Innovotek, and Silicon Valley Polytechnic Institute for their valuable support of this conference. Welcome to another stellar year of ISQED! It couldn't have happened without your support and participation.

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ISQED 2014 Best Papers

2B.6

Runtime 3-D Stacked Cache Data Management for Energy Minimization of 3-D Chip-Multiprocessors

Seunghan Lee[1], Kyungsu Kang[2], Jongpil Jung[1], Chong-Min Kyung[1]

[1]Korea Advanced Institute of Science and Technology, Korea,

[2]LSI Lab, EPFL, Lausanne, Switzerland

2C.1

Statistical Methodology for Modeling Non-IID Memory Fails Events

Sabine Francis[1], Rouwaida Kanj[1], Rajiv Joshi[2],

Ayman Kayssi[1], Ali Chehab[1]

[1]American University of Beirut, Beirut, Lebanon,

[2]IBM, Yorktown Heights, New York, USA

* Authors of best papers are honored during the luncheon on Tuesday March 4

ISQED 2014 FELLOW AWARD

Mark Budnik
Brandt Professor of Engineering and Department Chair
Valparaiso University

Citation:
Utmost Dedication to ISQED and Technical Excellence

Mark Budnik received his BS in electrical engineering from the University of Illinois and his MS and PhD in electrical engineering from Purdue University where he was the ECE Outstanding Graduate Student. He worked in the semiconductor industry for almost fifteen years before returning to academia. He is the Paul and Cleo Brandt Professor of Engineering and the Electrical and Computer Engineering Department Chair at Valparaiso University, Valparaiso, Indiana. He is the author of more than 60 book chapters and papers and has received four best paper/presentation awards. He is a senior member of the IEEE.

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ISQED 2014
GENERAL INFORMATION

March 3-5, 2014
Santa Clara Convention Center
5001 Great America Pkwy, Santa Clara, CA 95054

TUTORIALS

Monday Tutorials

Monday, March 3, 9:30am-6:00pm
Great America Meeting Room 3

Chair & Moderator:
Arijit Raychowdhury - *Georgia Institute of Technology*

Past, Present and Future of High Performance Logic Transistors

Prof. Suman Datta, *Pennsylvania State University*

.....

Integrated Techniques for Variation-Tolerant, Energy-Efficient Circuits

Dr. Carlos Tokunaga, *Intel Corporation*

.....

New Rules: Managing Processor Physics to Sustain Performance Scaling

Prof. Sudhakar Yalamanchili, *Georgia Tech*

.....

Very Large Scale Analog (VLSA): Synthesizing Cell-Based ADPLLs with Digital CAD Tools

Prof. David D. Wentzloff, *University of Michigan*

.....

CMOS Biosensors for Molecular Diagnostics and Cellular Monitoring

Prof Hua Wang, *Georgia Institute of Technology*

Emerging Materials for Energy Efficient Devices

Prof. Sayeef Salahuddin, *University of California at Berkeley*

KEYNOTE SPEECHES

Plenary Session 1P

Tuesday, March 4, 8:45am - 10:00am
Great America Ballroom

A New Era of Computing: Are You "Ready Now" To Build A Smarter and Secured Enterprise?

Jacqueline Woods
Global Vice President of Growth Solutions, STG
IBM

.....

Foundation for Trustworthy Platforms

Sridhar Iyengar
Director of Security and Privacy Research
Intel

ISQED LUNCHEON

Tuesday, March 4, 12:00pm-1:30pm
Great America Ballroom

ISQED AWARDS CEREMONY

Tuesday, March 4, 12:30pm-1:00pm
Great America Ballroom

ISQED Best Paper Awards

Recipients of the ISQED 2014 Best Paper Award will be recognized during the ISQED luncheon on Tuesday. List of best papers is shown in Page 2 of this document.

ISQED EXHIBITS

Tuesday, March 4, 3:00pm-7:00pm
Foyer Outside of Meeting Rooms 1, 2 and 3

GENERAL INFORMATION

KEYNOTE SPEECHES

Plenary Session 2P

Wednesday, March 5, 8:15am - 10:00am
Great America Ballroom

Cloud-Delivered Security for the Mobile Enterprise

Amit Sinha
EVP Engineering and Operations, Chief Technology Officer
Zscaler

Carbon Nanotube Computer: Transforming Scientific Discoveries into Working Systems

Subhasish Mitra
Professor and Director of the Robust Systems Group
Stanford University

Can You Trust the Internet of Things? A Look at Security of All Things Connected

Stacy Cannady
Technical Marketing - Trustworthy Computing TRIAD (Threat Response, Intelligence, and Development) for Cisco and a member of the Trusted Computing Group

TECHNICAL SESSIONS

There are a total of 18 technical sessions held on Tuesday and Wednesday. Technical sessions are held in the format of 3 parallel tracks in **Great America Meeting Rooms 1, 2 and 3**.

Poster Papers & Mixer

Poster display will take place on Tuesday afternoon 5:30pm-7:00pm in the Atrium area outside of **Great America Meeting Rooms 1, 2 and 3**. Authors will be available to discuss their works and to answer questions. Refreshments will be served.

ON-SITE REGISTRATION

Tentative time schedule of on-site registration is as follows:

Monday, March 3	*7:30am-4:00pm*
Tuesday, March 4	*8:00am-5:00pm*
Wednesday, March 5	*8:00am-1:00pm*

Registration desk location will be in the area beside Great America meeting rooms 1,2, and 3.

Co-located Events

IEDEC

4th Interdisciplinary Engineering Design & Education Conference

March 3
Great America Meeting Room 2
www.IEDEC.org

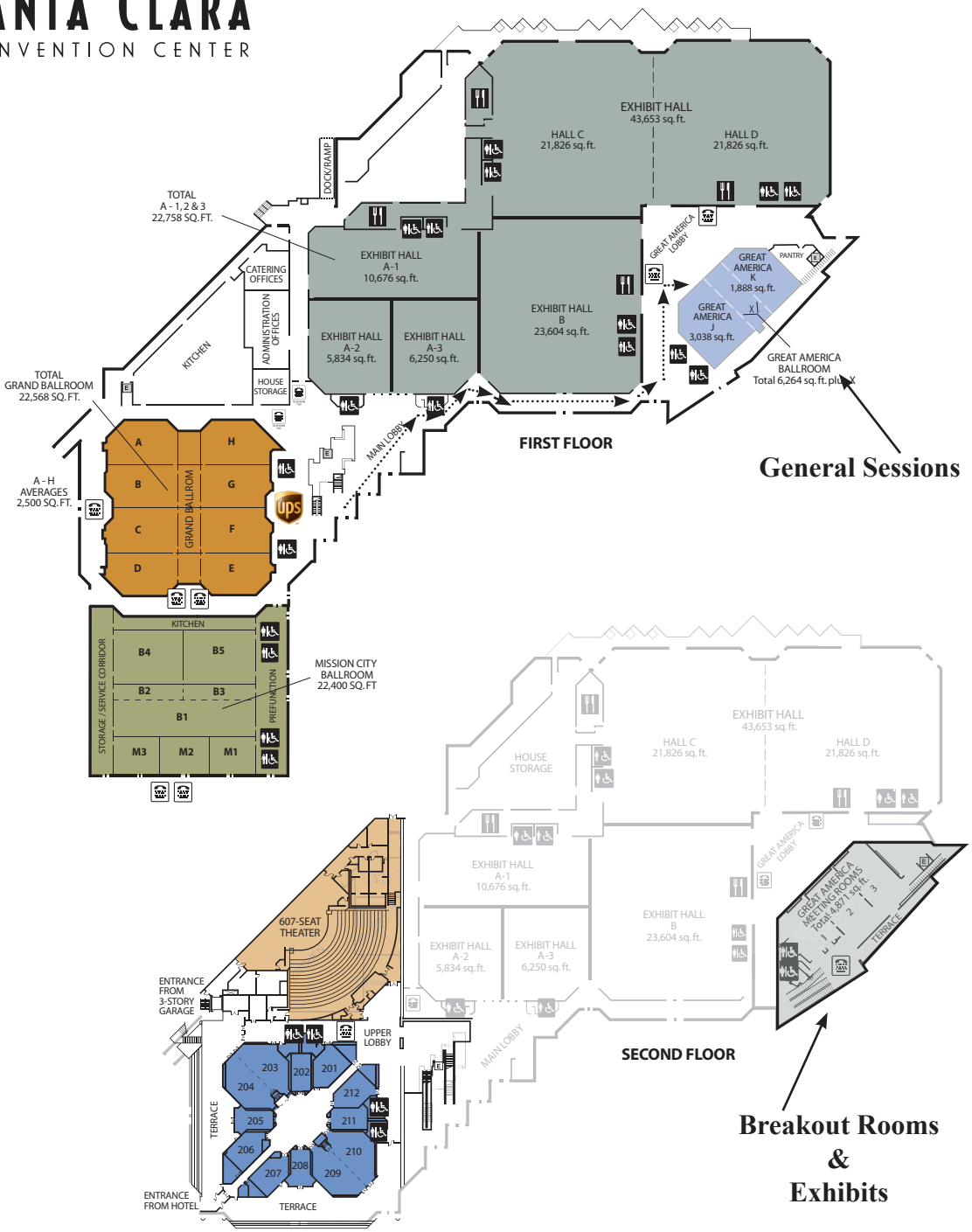
SensorsCon 2014

Sensors - Technology, Design, and Application Conference

March 6
Great America Meeting Room 2 and 3
www.SensorsCon.org

FLOOR PLAN

SANTA CLARA
CONVENTION CENTER



PROGRAM AT A GLANCE

ISQED 2014 PROGRAM AT A GLANCE

DATE	TIME			
MONDAY 3/3/2014	9:30AM-6:00PM	TUTORIALS BEST DESIGN PRACTICES FOR MODERN INTEGRATED CIRCUITS GREAT AMERICA MEETING ROOM 3		
TUESDAY 3/4/2014	8:45AM-10:00AM	PLENARY SESSION 1P (GREAT AMERICA BALLROOM) KEYNOTE SPEECHES BY: JACQUELINE WOODS - IBM , SRIDHAR IYENGAR -INTEL		
	10:00AM-10:20AM	MORNING BREAK		
	10:20AM-12:00PM	SESSION 1A MEMORY CIRCUIT AND SYSTEM GREAT AMERICA MEETING ROOM 1	SESSION 1B ADVANCED TECHNIQUES FOR SYSTEM-LEVEL ANALYSIS GREAT AMERICA MEETING ROOM 2	SESSION 1C NETWORK ON A CHIP AND MULTI-CORE SYSTEMS GREAT AMERICA MEETING ROOM 3
	12:00PM-12:45PM	ISQED LUNCHEON BEST PAPER AWARDS , COMMITTEE RECOGNITION AWARDS (GREAT AMERICA BALLROOM)		
	1:30PM-3:30PM	SESSION 2A VALIDATION AND SOC VERIFICATION GREAT AMERICA MEETING ROOM 1	SESSION 2B PACKAGE AND 3-D INTEGRATION GREAT AMERICA MEETING ROOM 2	SESSION 2C MANUFACTURING AND MODELING ISSUES IN NANOSCALE CMOS GREAT AMERICA MEETING ROOM 3
	3:30PM-3:50PM	AFTERNOON BREAK		
	3:50PM-5:30PM	SESSION 3A LOW VOLTAGE AND LOW POWER DESIGN METHODOLOGIES GREAT AMERICA MEETING ROOM 1	SESSION 3B SYSTEMS OPTIMIZATION GREAT AMERICA MEETING ROOM 2	SESSION 3C NOVEL TECHNOLOGIES AND THEIR APPLICATIONS GREAT AMERICA MEETING ROOM 3
	5:30PM-7:00PM	POSTER PAPERS & MIXER HALLWAY OUTSIDE GREAT AMERICA MEETINGS ROOMS		
WEDNESDAY 3/5/2014	8:15AM-10:00AM	PLENARY SESSION 2P (GREAT AMERICA BALLROOM) KEYNOTE SPEECHES BY: AMIT SINHA - ZSCALER, SUBHASISH MITRA - STANFORD UNIVERSITY, STACY CANNADY - TCG		
	10:00AM-10:20AM	MORNING BREAK		
	10:20AM-12:00PM	SESSION 4A RELIABILITY AND AGING GREAT AMERICA MEETING ROOM 1	SESSION 4B ADVANCES IN TIMING CLOSURE AND YIELD/RELIABILITY IMPROVEMENT GREAT AMERICA MEETING ROOM 2	SESSION 4C NEW IDEAS IN CIRCUIT DESIGN GREAT AMERICA MEETING ROOM 3
	12:00PM-1:30PM	LUNCH BREAK		
	1:30PM-3:30PM	SESSION 5A NOVEL TECHNOLOGIES, DESIGN & MODELINGGREAT AMERICA MEETING ROOM 1	SESSION 5B ASSERTION AND FORMAL VERIFICATION TECHNOLOGIES GREAT AMERICA MEETING ROOM 2	SESSION 5C THERMAL AND ENERGY CONSIDERATIONS IN SYSTEMS GREAT AMERICA MEETING ROOM 3
	3:30PM-3:50PM	AFTERNOON BREAK		
	3:50PM-5:30PM	SESSION 6A ADVANCED CIRCUIT AND SYSTEM METHODOLOGIES GREAT AMERICA MEETING ROOM 1	SESSION 6B POWER GRID ANALYSIS AND ISSUES GREAT AMERICA MEETING ROOM 2	SESSION 6C SMART SENSORS DESIGN TECHNOLOGY GREAT AMERICA MEETING ROOM 3

VENDOR EXHIBITS - 3:00PM-7:00PM

MONDAY TUTORIALS

Monday, March 3, 2014
9:30AM~6:00PM
Great America Meeting Room 3

Best Design Practices for Modern Integrated Circuits

Chair & Moderator
Prof. Arijit Raychowdhury - Georgia Institute of Technology

Presenters
Prof. Suman Datta - Pennsylvania State University
Dr. Carlos Tokunaga - Intel Corporation
Prof. Sudhakar Yalamanchili - Georgia Institute of Technology
Prof. David D. Wentzloff , University of Michigan
Prof. Hua Wang - Georgia Institute of Technology
Prof. Sayeef Salahuddin - University of California at Berkeley

Tutorial 1
9:30AM-10:40AM

Past, Present and Future of High Performance Logic Transistors

Presenter
Prof. Suman Datta, *Pennsylvania State University*

Energy efficient CMOS technology scaling per Moore's law demands a) continued electrostatic improvement; c) channel transport enhancement and, likely, c) new switching mechanism Strained silicon channel and high-k/metal gate stacks have enabled CMOS technology scaling for the past decade. With no room left for further scaling of the gate oxide thickness or junction engineering, the device community is left only with scaling of body thicknesses of field effect transistors to improve electrostatics. We will present state of the art and future FinFET technologies where silicon fins are likely to be replaced with Germanium, compound semiconductor (III-V) materials and their heterostructures. The impact of fin thickness scaling and quantum mechanical confinement on the electrostatics, performance and variation in such devices will be presented and its implication for super threshold and near threshold computing. Further scaling of supply voltage requires new switching mechanism like band to band tunneling for high ON current and sub-thermal switching slope devices. We will discuss recent progress on compound semiconductor based Tunnel FETs (TFETs) and their impact on energy-delay performance of logic and memory circuits. We will present a holistic device-circuit-system design strategy to take advantage of TFET device technology. Very recently, two-dimensional (2D) layered transition metal dichalcogenide materials (MX2) (M = Mo, W; X = S, Se, Te) have recently emerged as alternatives to III-Vs as channel materials for CMOS devices. Due to the very low value of the characteristic screening length (λ), these MX2 may give advantages over traditional 3D semiconductors for future tunnel field effect transistor applications.

Tutorial 2
10:50AM-12:00PM

Integrated Techniques for Variation-Tolerant, Energy-Efficient Circuits

Presenter
Dr. Carlos Tokunaga, *Intel Corporation*

The demand for high-performance operation in extremely power-constrained platforms such as smart phones and tablets requires architecture and circuit techniques that scale from efficient operation at low voltage to high performance when needed. It is well-known that energy efficiency improves as supply voltage is scaled down. Achieving this voltage reduction requires techniques that address intrinsic VMIN limitations in arrays (SRAM, register file arrays, ROMs), voltage, temperature and reliability guard band reduction, as well as techniques for reducing leakage energy. It is important that these techniques, while providing energy-efficient operation at low voltage, do not impact high performance mode which can be critical for many compute-intensive workloads. This tutorial will explore design techniques used to achieve energy-efficiency and resiliency to variations and discuss the challenges of integrating these techniques in an SoC. Recent results will be presented from several general-purpose processor and graphics test chips.

Tutorial 3
1:00PM-2:10PM

New Rules: Managing Processor Physics to Sustain Performance Scaling

Presenter
Prof. Sudhakar Yalamanchili, *Georgia Tech*

As industry moves to increasingly small feature sizes, performance scaling will become increasingly dominated by the physics of the computing environment. There are fundamental trade-offs to be made at the micro architectural level between performance, energy/power, and reliability. We refer to the body of knowledge addressing the impact of physics on such system level metrics as the processor physics. New efforts are emerging that are targeting understanding, characterizing, and collaboratively managing the multi-physics and multi-scale (nanoseconds to milliseconds) transient interactions between the delivery, dissipation, and removal (cooling) of energy and their impact on system level performance. In particular, these tradeoffs must be driven by application workloads. This talk will describe how interacting physical phenomena can affect application driven micro architecture-level tradeoffs and lead to operational principles for energy-efficient multicore architectures. In particular, the talk will cover recent work on improved dynamic power management in a commodity heterogeneous processor.

Tutorial 4
2:10PM-3:20PM

Very Large Scale Analog (VLSA): Synthesizing Cell-Based ADPLLs with Digital CAD Tools

Presenter
Prof. David D. Wentzloff, *University of Michigan*

As CMOS processes scale and digital gates become faster, it is practical to implement precisely-timed digital circuits switching in the GHz range that are synthesized using standard cell libraries and digital IC design flows. In parallel, the number of design for manufacturability checks has grown at an exponential rate in recent scaled CMOS processes, making full-custom analog design of CMOS ICs more challenging and time-consuming. As a result, traditionally analog circuits, such as those for clock generation and analog/digital conversion, have moved towards mostly-digital designs, significantly leveraging accurate time control and digital signal processing. This tutorial will focus on design techniques for implementing cell-based, all-digital PLLs that are synthesized using digital CAD flows. Recent results will be presented from a 400MHz ADPLL designed for the WBAN standard, and a 150-500 kHz programmable clock generator for ultra-low power processors.

Tutorial 5

3:40PM-4:50PM

CMOS Biosensors for Molecular Diagnostics and Cellular Monitoring

Presenter

Prof Hua Wang, *Georgia Institute of Technology*

Complementary Metal–Oxide–Semiconductor (CMOS), as one of the most matured integrated circuit (IC) processes, has gained increasing attention among the biosensors and bioelectronics community. Advanced CMOS process provides high-performance signal receiving and generation, unparalleled on-chip computation, and low cost at a mass-production level. As a result, CMOS ICs naturally offer a powerful, versatile, and cost-competitive platform for implementing integrated biosensors. In this talk, we will review several common sensor modalities which have been successfully implemented in CMOS process to address low-cost high-throughput molecular diagnostics and cellular monitoring applications. In particular, CMOS-based magnetic biosensors, as an emerging sensing modality, will be discussed. Several different CMOS-based magnetic sensing schemes will be covered, and their trade-offs among various sensor performance metrics will be compared.

Tutorial 6

4:50PM-6:00PM

Emerging Materials for Energy Efficient Devices

Presenter

Prof. Sayeef Salahuddin, University of California at Berkeley

Driven by the need of energy efficiency and scaling, research in electronic devices in the recent years has focused heavily on new materials and new phenomena, in part to go beyond the capabilities enabled by traditional Si CMOS technology. In this talk, I shall discuss three examples: (i) Two dimensional semiconductors, (ii) Ferroelectric materials and (ii) Magnetic materials. All these material systems are currently receiving significant effort from researchers all over the world. In each case, I shall describe our own perspectives as to their potential use for next generation electronics. I shall also discuss specific examples where these materials could lead to applications otherwise difficult to obtain by traditional means.

KEYNOTE SPEECHES
Plenary Session 1P

Great America Ball Room
8:45AM-10:00AM

Keynote Speech 1P.1
Tuesday, March 4
9:00AM-9:30AM

A New Era of Computing: Are You "Ready Now" To Build A Smarter and Secured Enterprise?

Jacqueline Woods
Global Vice President of Growth Solutions, STG
IBM

We are experiencing fundamental changes in how we interact, live, work and succeed in business. To support the new paradigm, computing must be simpler, more responsive and more adaptive, with the ability to seamlessly move from monolithic applications to dynamic services, from structured data at rest to unstructured data in motion, from supporting standard device interfaces to supporting a myriad of new and different devices every day. IBM understands this need to integrate social, mobile, cloud and big data to deliver value for your enterprise, so join this discussion, and learn how IBM helps customers leverage these technologies for superior customer value.

About Jacqueline Woods

Ms. Woods is the Global Vice President of Systems Software and Growth Solutions for the IBM Corporation. In this role, she leads the organization's marketing for Cloud, Analytics and Technical Computing. She's also drives business development for Competitive Independent Software Vendors, such as SAP and leads the Transformation account strategy for the division. In total, this represents a portfolio totaling ~ $ 12B. In this role she creates "blueprints for growth" designed to profitably accelerate sales. By building partnerships among channels (direct, indirect, and online) and other constituents (sales, operations, etc.), she unifies teams for a singular winning purpose. Her collective experience and body of work includes consumer and enterprise organizations for the Communications Sector (Energy, Telco, Media & Entertainment), the Financial Sector (Retail Banking, Commercial and Insurance), Distribution Sector (Consumer Packaged and Retail) and the Industrial Sector (Chemical, Petroleum and Electronics). In each of her roles, she's specialized in helping C-level executives of Fortune 500 companies reach their goals through a designed approach,

which at its core is focused on understanding customer needs more effectively and driving growth based on those needs. These efforts have generated more than a billion dollar in revenue across the following sectors – Communications, Energy, Industrial, Transportation, and Financial Services. Ms. Woods was featured in Fortune Magazine's 50 Most Powerful Black Executives in America in 2003, Ebony's Top 15 Women in Business in America in 2004, and Black Enterprise's Top 50 Black Female Executives in February 2006. She's also been featured in the NY Times and Wall Street Journal. She's also presented at Harvard, the Kennedy School of Government, the Organization for Cooperative Economic Development, and various customer experience and marketing conferences. Ms. Woods is a Merit Fellow and holds an MBA from the University of Southern California, Marshall School of Business, with a concentration in marketing and venture management. She holds a BS from the University of California, Davis in Managerial Economics. She also served as member of the Dean's Council for the Kennedy School of Government, Harvard University from 2003-2009.

Keynote Speech 1P.2

Tuesday, March 4
9:30AM-10:00AM

Foundation for Trustworthy Platforms

Sridhar Iyengar
Director of Security and Privacy Research
Intel

In the last decade, malware attacks on our platforms have exploded in frequency, sophistication and virulence. Billions of smart devices connect to servers in the cloud, all transporting, processing and storing our most sensitive data. All this forms a large threat surface that is becoming increasingly hard to protect against a determined adversary. This talk will address key security research leading to silicon features on Intel platforms. These provide a strong foundation to proactively combat malware; provide the necessary acceleration for encryption and enhancements for better isolation and data protection. The talk will also address how software can and should take advantage of the hardware features to address the challenges of security in a connected world.

About Sridhar Iyengar

Sridhar has been at Intel for 30 years in various technical, research and managerial capacities, both in the labs and product groups. He is currently the Director of Security and Privacy Research, a group that is chartered to drive game-changing technologies to make "trustworthiness" a fundamental aspect of Intel platforms. He holds a Bachelor of Technology in Electrical Engineering from IIT Madras and a Masters in Computer Science from the University of Wisconsin, Madison.

SESSION 1A

Tuesday March 4, 2014

Great America Meeting Room 1

Memory Circuit and System

Chair: **Stephen Heinrich-Barna**, Texas Instruments
Co-Chair: **Saibal Mukhopadhyay**, Georgia Tech

10:20AM
1A.1
A Reverse Write Assist Circuit for SRAM Dynamic Write VMIN Tracking using Canary SRAMs
Arijit Banerjee[1], Mahmut E. Sinangil[2], John Poulton[2], C. Thomas Gray[2], Benton H. Calhoun[1]
[1]University of Virginia, [2]NVIDIA

10:40AM
1A.2
Exploiting Static and Dynamic Locality of Timing Errors in Robust L1 Cache Design
Hu Chen, Sanghamitra Roy, Koushik Chakraborty
Utah State University

11:00AM
1A.3
A 40-nm Resilient Cache Memory for Dynamic Variation Tolerance with Bit-Enhancing Memory and On-Chip Diagnosis Structures Delivering ×91 Failure Rate Improvement
Yohei Nakata[1], Yuta Kimi[1], Shunsuke Okumura[1], Jinwook Jung[1], Takuya Sawada[1], Taku Toshikawa[1], Makoto Nagata[2], Hirofumi Nakano[3], Makoto Yabuuchi[3], Hidehiro Fujiwara[3], Koji Nii[3], Hiroyuki Kawai[3], Hiroshi Kawaguchi[1], Masahiko Yoshimoto[2]
[1]Kobe University, [2]Kobe University, JST CREST, [3]Renesas Electronics Corporation

11:20AM
1A.4
40nm ultra-low leakage SRAM at 170 deg.C operation for embedded flash MCU
Yoshisato Yokoyama, Yuichiro Ishii, Hidemitsu Kojima, Atsushi Miyanishi, Yoshiki Tsujihashi, Shinobu Asayama, Kazutoshi Shiba, Koji Tanaka, Tatsuya Fukuda, Koji Nii, Kazumasa Yanagisawa
Renesas Electronics Corporation

11:40AM
1A.5
Impact of Proactive Reconfiguration Technique on Vmin and Lifetime of SRAM Caches
Peyman Pouyan, Esteva Amat, Enrique Barajas, Antonio Rubio
Department of Electronic Engineering UPC Barcelona Tech

SESSION 1B

Tuesday March 4, 2014

Great America Meeting Room 2

Advanced Techniques for System-level Analysis

Chair: **James Lei**, Omnivision

10:20AM
1B.1
Modeling, Design and Verification Platform using SystemC AMS
Yao Li, Ramy Iskander, Marie-Minerve Louërat
UPMC-LIP6

10:40AM
1B.2
On Application of One-class SVM to Reverse Engineering-Based Hardware Trojan Detection
Chongxi Bao[1], Domenic Forte[2], Ankur Srivastava[1]
[1]University of Maryland, [2]University of Connecticut

11:00AM
1B.3
Employing a Timed Colored Petri Net to Achieve an Accurate Model for NoC Performance Evaluation
César Marcon[1], Jarbas Silveira[2], Paulo Cortez[2], Giovani Barroso[3]
[1]PPGCC / PUCRS, [2]LESC-DETI / UFC, [3]UFC

11:20AM
1B.4
Integrated Particle Swarm Optimization (i-PSO): An Adaptive Design Space Exploration Framework for Power-Performance Tradeoff in Architectural Synthesis
Anirban Sengupta and Vipul Kumar Mishra
Indian Institute of Technology - IIT Indore

11:40AM
1B.5
Modeling and Analysis of System Stability in a Distributed Power Delivery Network with Embedded Digital Linear Regulators
Saad Bin Nasir, Youngtak Lee, Arijit Raychowdhury
Georgia Institute of Technology

SESSION 1C

Tuesday March 4, 2014

Great America Meeting Room 3

Network on a Chip and Multi-core Systems

Chair: **Rajesh Berigei**, Texas Instruments
Co-Chair: **Jose Matos**, University of Porto, Portugal

10:20AM
1C.1
An Application-Aware Heterogeneous Prioritization Framework for NoC-based Chip Multiprocessors
Tejasi Pimpalkhute and Sudeep Pasricha
Colorado State University

10:40AM
1C.2
Adding virtualization support in MIPS 4Kc-based MPSoCs
Alexandra Aguiar, Carlos Moratelli, Marcos Sartori, Fabiano Hessel
PUCRS

11:00AM
1C.3
HELIX: Design and Synthesis of Hybrid Nanophotonic Application-Specific Network-On-Chip Architectures
Shirish Bahirat and Sudeep Pasricha
Department of Electrical and Computer Engineering Colorado State University

11:20AM
1C.4
An Analytical Approach to System-level Variation Analysis and Optimization for Multi-core Processors
Chenyun Pan, Saibal Mukhopadhyay, Azad Naeemi
Georgia Institute of Technology

11:40AM
1C.5
Heterogeneity Exploration for Peak Temperature Reduction on Multi-Core Platforms
Tianyi Wang[1], Ming Fan[1], Gang Quan[1], Shangping Ren[2]
[1]Florida International University, [2]Illinois Institute of Technology

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ISQED Luncheon

Tuesday March 4
Great America Ball Room
12:00PM-1:30PM

ISQED 2014 Award Ceremony

12:30PM-1:00PM

Best Paper Award
Recognition Award

SESSION 2A

Tuesday March 4, 2014

Great America Meeting Room 1

Validation and SOC Verification

Chair: **Sreejit Chakravarty**, LSI Corporation
Co-Chair: **Senthil Arasu**, Broadcom

1:30PM
2A.1
Efficient Post-Silicon Validation via Segmentation of Process Variation Envelope – Global vs Local Variations
Prasanjeet Das[1] and Sandeep Gupta[2]
[1]Oracle America Inc., [2]University of Southern California

1:50PM
2A.2
Protection of Muller-Pipelines from Transient Faults
Syed Rameez Naqvi, Jakob Lechner, Andreas Steininger
Vienna University of Technology

2:10PM
2A.3
Runtime Fault Recovery Protocol for NoC-based MPSoCs
eduardo wachter, augusto erichsen, leonardo juracy, alexandre amory, fernando moraes
PUCRS

2:30PM
2A.4
Concurrency-Oriented SoC Re-Certification by Reusing Block-Level Test Vectors
Hsuan-Ming Chou, Hong-Chang Wu, Yi-Chiao Chen, Shih-Chieh Chang
National Tsing Hua University

2:50PM
2A.5
Efficient Trace Signal Selection using Augmentation and ILP Techniques
Kamran Rahmani[1], Prabhat Mishra[1], Sandip Ray[2]
[1]University of Florida, [2]Intel Corporation

3:10PM
2A.6
Directed Test Generation for Hybrid Systems
Sudhi Proch and Prabhat Mishra
University Of Florida

SESSION 2B

Tuesday March 4, 2014

Great America Meeting Room 2

Package and 3-D Integration

Chair: **Farhang Yazdani**, Broadpak
Co-Chair: **Srinivas Bodapati**, Intel

1:30PM
2B.1
Temperature-Aware Runtime Power Management for Chip-Multiprocessors with 3-D Stacked Cache
Kyungsu Kang[1], Seunghan Lee[2], Giovanni De Micheli[3], Chong-Min Kyung[2]
[1]Samsung, [2]KAIST, [3]EPFL

1:50PM
2B.2
Efficient Region-Aware P/G TSV Plannng for 3D ICs
Song Yao[1], Xiaoming Chen[1], Yu Wang[1], Yuchun Ma[2], Yuan Xie[3], Huazhong Yang[1]
[1]Dept. of E.E., TNList, Tsinghua Univ., China, [2]Dept. of C.S., TNList, Tsinghua Univ., China, [3]Computer Science and Engr. Dept, Pennsylvania State University, U.S.A.

2:10PM
2B.3
3D-ICs with Self-Healing Capability for Thermal Effects in RF Circuits
Abhilash Goyal[1], Madhavan Swaminathan[2], Abhijit Chatterjee[2]
[1]IEEE Member Student at San Jose State, [2]Professor at GaTech

2:30PM
2B.4
Comparative Analysis of Clock Distribution Networks for TSV-based 3D IC Designs
Mir mohammad Navidi and Gyung-Su Byun
West Virginia University

2:50PM
2B.5
Delay and Power Optimization with TSV-aware 3D Floorplanning
Mohammad Ahmed and Malgorzata Chrzanowska-Jeske
Portland State University

3:10PM
2B.6
Runtime 3-D Stacked Cache Data Management for Energy Minimization of 3-D Chip-Multiprocessors
Seunghan Lee[1], Kyungsu Kang[2], Jongpil Jung[1], Chong-Min Kyung[1]
[1]EE, Korea Advanced Institute of Science and Technology, Daejeon, Korea, [2]LSI, EPFL, Lausanne, Switzerland

SESSION 2C

Tuesday March 4, 2014

Great America Meeting Room 3

Manufacturing and Modeling Issues in Nanoscale CMOS

Chair: **Brian Cline**, ARM
Co-Chair: **Srini Krishnamoorthy**, AMD

1:30PM
2C.1
Statistical Methodology for Modeling Non-IID Memory Fails Events
Sabine Francis[1], Rouwaida Kanj[1], Rajiv Joshi[2], Ayman Kayssi[1], Ali Chehab[1]
[1]American University of Beirut, [2]IBM TJ Watson Labs

1:50PM
2C.2
Automated Shmoo Data Analysis: A Machine Learning Approach
Wei Wang
Intel Corporation

2:10PM
2C.3
Double Patterning-Aware Detailed Routing with Mask Usage Balancing
Seong-I Lei[1], Chris Chu[2], Wai-Kei Mak[1]
[1]National Tsing Hua University, [2]Iowa State University

2:30PM
2C.4
Design of Radiation Hardened Wide Tuning Range CMOS Oscillators
Sharayu Jagtap, Sivaramakrishna R, Shalabh Gupta
Indian Institute of Technoloogy Bombay

2:50PM
2C.5
Computer Simulation of Radiation-Induced Clock-Perturbation in Phase-Locked Loop with Analog Behavioral Model
Tomohiro FUJITA[1], SinNyoung KIM[2], Hidetoshi ONODERA[2]
[1]Ritsumeikan University, [2]Kyoto University

3:10PM
2C.6
Measuring SET Pulsewidths in Logic Gates using Digital Infrastructure
Varadan Savulimedu Veeravalli, Andreas Steininger, Ulrich Schmid
Vienna University of Technology

SESSION 3A

Tuesday March 4, 2014

Great America Meeting Room 1

Low Voltage and Low Power Design Methodologies

Chair: **Visvesh Sathe**, Univerity of Washington Seatle
Co-Chair: **Saibal Mukhopadhyay**, Georgia Tech

3:50PM
3A.1
Fast, Accurate Variation-Aware Path Timing Computation for Sub-threshold Circuits
Yanqing Zhang and Benton Calhoun
University of Virginia

4:10PM
3A.2
An Improved Logical Effort Model and Framework Applied to Optimal Sizing of Circuits Operating in Multiple Supply Voltage Regimes
Xue Lin, Yanzhi Wang, Shahin Nazarian, Massoud Pedram
University of Southern California

4:30PM
3A.3
Sub-threshold Custom Standard Cell Library Validation
Bo Liu[1], Maryam Ashouei[2], Tobias Gemmeke[2], Jose Pineda de Gyvez[1]
[1]Electronic Systems, Electrical Engineering, Technische Univ. Eindhoven, Eindhoven, NL, [2]Holst Centre/imec-nl, Eindhoven, NL

4:50PM
3A.4
Power and Area-Efficient Approximate Wallace Tree Multiplier for Error-Resilient Systems
Kartikeya Bhardwaj[1], Pravin Mane[2], Joerg Henkel[3]
[1]Electrical & Electronics Engineering, BITS Pilani-Goa Campus, Goa-403726, India, [2]Electrical & Electronics Engineering, BITS Pilani – Goa Campus Goa -403726 India, [3]Department of Computer Science, Karlsruhe Institute of Technology, Karlsruhe, Germany

5:10PM
3A.5
Predictive Synchronization for DVFS-Enabled Multi-Processor Systems
Mark Buckler and Wayne Burleson
UMass Amherst, AMD Research

SESSION 3B

Tuesday March 4, 2014

Great America Meeting Room 2

Systems Optimization

Chair: **Sudeep Pasricha**, Colorado State Univ
Co-Chair: **Houman Homayoun**, George Mason University

3:50PM
3B.1
Ring-based Sharing Fabric for Efficient Pipelining of Kernel-Stream on CGRA-based Multi-Core Architecture
Heesun Kim, Seungyun Sohn, Yoonjin Kim
Department of Computer Science, Sookmyung Women's University

4:10PM
3B.2
Multi-Core Partitioned Scheduling For Fixed-Priority Periodic Real-Time Tasks With Enhanced RBound
Ming Fan[1], Qiushi Han[2], Gang Quan[1], Shangping Ren[3]
[1]Florida International University, [2]Florida International Unversity, [3]Illinois Institute of Technology

4:30PM
3B.3
Minimizing Clock Domain Crossing in Network on Chip Interconnect
Parag Kulkarni[1], Puneet Gupta[2], Rudy Beraha[3]
[1]Synopsys, [2]UCLA, [3]Qualcomm

4:50PM
3B.4
Optimal Reliability-Constrained Overdrive Frequency Selection In Multicore Systems
Andrew B. Kahng and Siddhartha Nath
University of California, San Diego

5:10PM
3B.5
RTL Datapath Optimization Using System-level Transformations
Samaneh Ghandali[1], Bijan Alizadeh[1], Masahiro Fujita[2], Zainalabedin Navabi[1]
[1]School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran, [2]VLSI Design and Education Center (VDEC), University of Tokyo, Tokyo, Japan

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SESSION 3C

Tuesday March 4, 2014

Great America Meeting Room 3

Novel Technologies and their Applications

Chair: **Paul Tong**, Pericom
Co-Chair: **Bao Liu**, University of Texas, San Antonio

3:50PM
3C.1
Dual-sided Doped Memristor and Its SPICE Modeling for Improved Electrical Properties
Anup Shrivastava[1] and Jawar Singh[2]
[1]IIITDM, Jabalpur, [2]IIITDM,Jabalpur

4:10PM
3C.2
Linearly Separable Pattern Classification Using Memristive Crossbar Circuits
Komal Singh, Chitrakant Sahu, Jawar Singh
Indian Institute of Information Technology Design and Manufacturing, Jabalpur, India

4:30PM
3C.3
Low-power programmable-logic array using nonvolatile complementary atom switch
Makoto Miyamura, Toshitsugu Sakamoto, Munehiro Tada, Naoki Banno, Koichi Okamoto, Noriyuki Iguchi, Hiromitsu Hada
LEAP

4:50PM
3C.4
Volume Accumulated Double Gate Junctionless MOSFETs for Low Power Logic Technology Applications
Mukta Singh Parihar and Abhinav Kranti
Indian Institute of Technology Indore (IITI), India

5:10PM
3C.5
Stack Sizing Analysis and Optimization for FinFET Logic Cells and Circuits Operating in the Sub/Near-Threshold Regime
Xue Lin, Yanzhi Wang, Massoud Pedram
University of Southern California

Poster Session & Mixer

Tuesday March 4, 2014

5:30PM – 7:00PM

Chair: **Peter Wright**, Synopsys
Co-Chair: **Syed M Alam**, Everspin Technologies

P.1
A Parallel Clustering Algorithm for Placement
Amir Momeni, Perhaad Mistry, David Kaeli
Department of Electrical and Computer Engineering, Northeastern University

P.2
An Optimization Algorithm for Simultaneous Routing and Buffer Insertion with Delay-Power Constraints in VLSI Layout Design
Chessda Uttraphan[1], Nasir Shaikh-Husin[2], Mohamed Khalil-Hani[2]
[1]Universiti Tun Hussein Onn Malaysia (UTHM), [2]Universiti Teknologi Malaysia (UTM)

P.3
Kriging Bootstrapped Neural Network Training for Fast and Accurate Process Variation Analysis
Oghenekarho Okobiah, Saraju Mohanty, Elias Kougianos
University of North Texas, Denton

P.4
Design and Analysis of a Touch Mode MEMS Capacitive Pressure Sensor for IUPC
Anil sharma and Jawar Singh
IIITDM Jabalpur

P.5
Impedance Modeling of Intracortical Microelectrode for a Reliable Design of Brain Activity Recording System
Daniela De Venuto[1], Peter Ledochowitsch[2], Michel Maharabitz[2], Jan Rabaey[2]
[1]Politecnico di Bari, Italy, [2]UC Berkeley (CA) USA

P.6
Direct Finite-Element-Based Solver for 3D-IC Thermal Analysis via H-Matrix Representation
Ying Chi Li[1], Sheldon X.-D. Tan[2], Tan Yu[2], Xin Huang[2], Ngai Wong[1]
[1]The University of Hong Kong, [2]University of California, Riverside

P.7
Compiler-Directed Leakage Energy Reduction for Instruction Scratch-Pad Memories
Yijie Huangfu and Wei Zhang
Virginia Commonwealth University

P.8
Fast Design Space Subsetting for Configurable Caches
Mohamad Hammam Alsafrjalani[1], Ann Gordon-Ross[1], Pablo Viana[2]
[1]University of Florida, [2]Federal University of Alagoas, FEAC dept., Brazil

P.9
A Framework for MPSoC Generation and Distributed Applications Evaluation
Guilherme Machado de Castilhos, Eduardo Weber Wachter, Guilherme Afonso Madalozzo, Augusto Gosmann Erichsen, Thiago Mânica Monteiro, Fernando Gehm Moraes
PUCRS

P.10
Architecture for Monitoring SET Propagation in 16-bit Sklansky Adder
Varadan Savulimedu Veeravalli and Andreas Steininger
Vienna University of Technology, Austria

P.11
Towards more Reliable Embedded Systems through a Mechanism for Monitoring Driver Devices Communication
Rafael Melo Macieira, Edna Barros, Camila Ascendina
CIn/UFPE

P.12
Experimental validation of minimum operating-voltage-estimation for low supply voltage circuits
Takashi Sato[1], Junya Kawashima[1], Hiroshi Tsutsui[2], Hiroyuki Ochi[3]
[1]Kyoto University, [2]Hokkaido University, [3]Ritsumeikan University

P.13
Application of Six-Sigma DMAIC Methodology in the Evaluation of Test Effectiveness: A Case Study for EDA Tools
Eman El Mandouh
Quality Assurance Manager for Questa Formal Tools

P.14
Systematic Analyses for Latching Probability of Single-Event Transients
Hoda Pahlevanzadeh and Qiaoyan Yu
University of New Hampshire

P.15
GPU-Accelerated Sparse Matrix-Vector Multiplication For Fast Transient Thermal Analysis
Kai He[1], Tan Yu[1], Sheldon Tan[1], Hai Wang[2], He Tang[2]
[1]University of California, Riverside, [2]UESTC

KEYNOTE SPEECHES

Plenary Session 2P

Wednesday March 5
Great America Ball Room
8:15AM-10:00AM

Keynote Speech 2P.1
Wednesday, March 5
8:30AM-9:00AM

Cloud-Delivered Security for the Mobile Enterprise

Amit Sinha
EVP Engineering and Operations, Chief Technology Officer
Zscaler

The adoption of Mobility, Cloud and Social Media is driving businesses to spend more on the deployment of costly appliance-based point solutions for Internet security that still leave significant gaps in coverage. Appliances also accrue additional costs due to administration overhead and backhauling of traffic to a central locations for inspection and policy enforcement. Cloud-delivered security can provide a safe and rich Internet experience for users on any device at any location, without requiring organizations to manage any hardware or software. Enterprises can eliminate appliance and backhauling costs by enabling their traffic to directly go to the Internet via a Security Cloud. This talk will focus on how to build and run a global Security Cloud that can protect millions of users across thousands of organizations.

About Amit Sinha

Dr. Amit Sinha is skilled entrepreneur and leader, having driven research and development of disruptive security and wireless technologies for multiple market-leading organizations, including Zscaler, Motorola, AirDefense and Engim. At Zscaler, Sinha is responsible for all engineering and operations of Zscaler's Security Cloud—from product design, development, testing to managing and scaling the cloud. Sinha earned his MS and PhD in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology and his B.Tech. in Electrical Engineering from the Indian Institute of Technology, Delhi where he was awarded the President of India Gold Medal for graduating summa cum laude. He holds 27 US patents and has contributed to three books and dozens of conference and journal papers.

Keynote Speech 2P.2

Wednesday, March 5
9:00AM-9:30AM

Carbon Nanotube Computer: Transforming Scientific Discoveries into Working Systems

Subhasish Mitra
Professor and Director of the Robust Systems Group
Stanford University

Carbon Nanotube Field Effect Transistors (CNFETs) are excellent candidates for building highly energy-efficient future electronic systems. Unfortunately, carbon nanotubes (CNTs) are subject to substantial inherent imperfections that pose major obstacles to the design of robust and very large-scale CNFET digital systems: It is nearly impossible to guarantee perfect alignment and positioning of all CNTs. This limitation introduces stray conducting paths, resulting in incorrect circuit functionality. CNTs can be metallic or semiconducting depending on chirality. Metallic CNTs cause shorts resulting in excessive leakage and incorrect circuit functionality. A combination of design and processing techniques overcomes these challenges by creating robust CNFET digital circuits that are immune to these inherent imperfections. This imperfection-immune design paradigm enables the first experimental demonstration of the carbon nanotube computer, and, more generally, arbitrary digital systems that can be built using CNFETs. Monolithically integrated three-dimensional CNFET circuits will also be discussed. This research was performed at Stanford University in collaboration with Prof. H.-S. Philip Wong and several graduate students.

About Subhasish Mitra

Professor Subhasish Mitra directs the Robust Systems Group in the Department of Electrical Engineering and the Department of Computer Science of Stanford University, where he is the Chambers Faculty Scholar of Engineering. Before joining Stanford, he was a Principal Engineer at Intel Corporation. Prof. Mitra's research interests include robust system design, VLSI design, CAD, validation and test, and emerging nanotechnologies. His X-Compact technique for test compression has been key to cost-effective manufacturing and high-quality testing of a vast majority of electronic systems, including numerous Intel products. X-Compact and its derivatives have been implemented in widely-used commercial Electronic Design Automation tools. The QED and IFRA techniques, created jointly with his students, have shown outstanding results in overcoming critical bottlenecks in post-silicon validation and debug for several commercial hardware platforms, and have been characterized as "breakthrough" in a Research Highlight in the Communications of the ACM. His work on carbon nanotube imperfection-immune digital VLSI, jointly with his students and collaborators, resulted in the demonstration of the first carbon nanotube computer, and it was featured on the cover of NATURE

(Sept. 2013). The National Science Foundation presented this work as a Research Highlight to the United States Congress, and it also was highlighted as "an important, scientific breakthrough" by the BBC, Economist, EE Times, IEEE Spectrum, MIT Technology Review, New York Times, Scientific American, Time, Wall Street Journal, Washington Post, and numerous other organizations worldwide. Prof. Mitra's major honors include the Presidential Early Career Award for Scientists and Engineers from the White House, the highest United States honor for early-career outstanding scientists and engineers, Terman Fellowship, and the Intel Achievement Award, Intel's highest corporate honor. He and his students published award-winning papers at major forums on a wide range of topics spanning robust systems, VLSI design, validation and test, and nanotechnologies: IEEE/ACM Design Automation Conference, IEEE International Test Conference, IEEE Trans. CAD, IEEE VLSI Test Symposium, Intel Design and Test Technology Conference, and the Symposium on VLSI Technology. At Stanford, he was honored several times by graduating seniors "for being important to them during their time at Stanford." Prof. Mitra has served on numerous conference committees and journal editorial boards. Recently, he served on DARPA's Information Science and Technology Board as an invited member. He is a Fellow of the IEEE.

Keynote Speech 2P.3

Wednesday, March 5
9:30AM-10:00AM

Can You Trust the Internet of Things? A Look at Security of All Things Connected

Stacy Cannady
Technical Marketing - Trustworthy Computing TRIAD (Threat Response, Intelligence, and Development) for Cisco and a member of the Trusted Computing Group

Once we worried about the security of our desktop computers. Then came increasingly powerful and connected mobile devices…which offered the keys to the kingdom to anyone willing to spend a bit of time attacking them. Now, in addition to our continuing concerns about devices we now see as powerful computers, we must look to securing the next generation of connected devices. But these devices don't fit on the desktop or even in the hand. They instead are scattered around the home, the office, the manufacturing plant, the retail store and even on the highway. Home appliances, cars, personal fitness devices, medical devices, factory automation systems, thermostats and security systems, even a smoke detector - these all fit in the Internet of Things. Therefore, security must be considered. This talk will address some key issues and core concepts of IoT security including the possible role of trust and use of existing and evolving industry standards. Attendees will get a new perspective on embedded strong security into a variety of devices. This session includes discussion of several security architectures already deployed in IoT devices and includes resources for the tools used to implement those architectures (mostly available for free).

About Stacy Cannady

Stacy Cannady, CISSP, is technical marketing - Trustworthy Computing TRIAD (Threat Response, Intelligence, and Development) for Cisco and a member of the Trusted Computing Group's Embedded Systems Work Group. He is an alternate board member representing Cisco. Stacy has worked in the field of trusted computing for a number of years. As a subject matter expert in trusted computing, his responsibilities require an in-depth understanding of the trusted computing market, including advances in hardware and software security as well as vendor and customer market dynamics. Prior to his work with Cisco, Stacy was responsible for marketing leadership for trusted computing at DMI, IBM and at Lenovo. At IBM, he played a principal role in making the TPM standard equipment in ThinkPad and ThinkCenter PCs. This created competitive pressure in the PC market and led to broad market acceptance of the TPM as standard equipment in enterprise-class PCs. Stacy was also responsible for

the security product strategy for IBM's PC Division and for Lenovo for eight years. This strategy required subject matter expertise in firmware security, biometrics, smart cards, identity management, encryption and access control. Additionally, at Lenovo, he was also responsible for incident response and served as Privacy Manager for the Software & Peripherals Business Unit.

SESSION 4A

Wednesday March 5, 2014

Great America Meeting Room 1

Reliability and Aging

Chair: **Rajiv Joshi**, IBM
Co-Chair: **Arijit Raychowdhury**, Georgia Tech

10:20AM
4A.1
Assessment of Reliability Impact on GHz Processors with Moderate Overdrive
Mitsuhiko Igarashi, Hideki Aono, Hideaki Abe, Koji Shibutani, Kan Takeuchi
Renesas Electronics Corporation

10:40AM
4A.2
Study of IC Aging on Ring Oscillator Physical Unclonable Functions
Dinesh Ganta and Leyla Nazhandali
Virginia Tech

11:00AM
4A.3
Circuit-level approach to improve the temperature reliability of Bi-stable PUFs
Dinesh Ganta and Leyla Nazhandali
Virginia Tech

11:20AM
4A.4
Degradation Analysis of Datapath Logic Subblocks under NBTI Aging in FinFET Technology
Halil Kukner[1], Moustafa Khatib[2], Sebastien Morrison[2], Pieter Weckx[1], Praveen Raghavan[2], Ben Kaczer[2], Francky Catthoor[1], Liesbet Van der Perre[1], Rudy Lauwereins[1], Guido Groeseneken[1]
[1]imec,KUL, [2]imec

11:40AM
4A.5
Fine Grained Wearout Sensing using Metastability Resolution Time
Vikram Suresh and Wayne Burleson
University of Massachusetts, Amherst

SESSION 4B

Wednesday March 5, 2014

Great America Meeting Room 2

Advances in Timing Closure and Yield/Reliability Improvement

Chair: **Vamsi Srikantam**, Veloce Technologies

10:20AM
4B.1
Methodology to Optimize Critical Node Seperation in Hardened Flip-Flops
Sandeep Shambhulingaiah, Srivatsan Chellappa, Sushil Kumar, Lawrence Clark
Arizona State University

10:40AM
4B.2
Asymmetric Aging of Clock Networks in Power Efficient Designs
Senthil Arasu[1], Mehrdad Nourani[1], Frank Cano[2], John Carulli[2], Vijay Reddy[2]
[1]University of Texas at Dallas, [2]Texas Instruments Inc

11:00AM
4B.3
Post-Silicon Tunable Clock Buffer Allocation Based on Fast Chip Yield Computation
Hyungjung Seo[1] and Taewhan Kim[2]
[1]School of Electrical Engineering and Computer Science, Seoul National University, Seoul, Korea, [2]Nano Systems Institute (NSI), Seoul National University, Seoul, Korea

11:20AM
4B.4
Timing Margin Recovery With Flexible Flip-Flop Timing Model
Andrew B. Kahng and Hyein Lee
UC San Diego

11:40AM
4B.5
NOLO : A No-Loop, Predictive Useful Skew Methodology for Improved Timing in IC Implementation
Tuck-Boon Chan, Andrew B. Kahng, Jiajia Li
UCSD

SESSION 4C

Wednesday March 5, 2014

Great America Meeting Room 3

New Ideas in Circuit Design

Chair: **Miroslav Velev**, Aries Design Automation
Co-Chair: **Anand Iyer**, AMD

10:20AM
4C.1
Constructing Small-Signal Equivalent Impedances Using Ellipsoidal Norms
Sandeep Koranne
Mentor Graphics Corporation

10:40AM
4C.2
Sense Amplifier Pass Transistor Logic For Energy Efficient and DPA-Resistant AES Circuit
Mehrdad Khatir and leyla Nazhandali
Virginia Tech

11:00AM
4C.3
Assessing Uniqueness and Reliability of SRAM-based Physical Unclonable Functions from Silicon Measurements in 45-nm bulk CMOS
Hidehiro Fujiwara, Makoto Yabuuchi, Koji Nii
Renesas Electronics Corporation

11:20AM
4C.4
TASSER: A Temperature-Aware Statistical Soft-Error-Rate Analysis Framework for Combinational Circuits
Sung S.-Y. Hsueh, Ryan H.-M. Huang, Charles H.-P. Wen
Department of Electrical and Computer Engineering, National Chiao Tung University

11:40AM
4C.5
PETS: Power and Energy Estimation Tool at System-Level
Santhosh Kumar Rethinagiri[1], Oscar Palomar[2], Rabie Ben Atitallah[3], Adrian Cristal[2], Osman Unsal[2], Smail Niar[3]
[1]BSC-Microsoft Research Center, [2]Barcelona Supercomputing Center, [3]University of Valenciennes

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SESSION 5A

Wednesday March 5, 2014

Great America Meeting Room 1

Novel Technologies, Design & Modeling

Chair: **Paul Tong**, Pericom
Co-Chair: **Bao Liu**, University of Texas, San Antonio

1:30PM
5A.1
Impact of FinFET Technology for Power Gating in Nano-Scale Design
Keunwoo Kim[1], Rouwaida Kanj[2], Rajiv Joshi[3]
[1]Samsung, [2]American University of Beirut, [3]IBM TJ Watson

1:50PM
5A.2
Avoiding Unnecessary Write Operations in STT-MRAM for Low Power Implementation
Rajendra Bishnoi, Fabian Oboril, Mojtaba Ebrahimi, Mehdi Tahoori
Karlsruhe Institue of Technology

2:10PM
5A.3
A Workload-Aware-Design of 3D-NAND Flash Memory for Enterprise SSDs
Chao Sun[1], Ayumi Soga[2], Takahiro Onagi[2], Koh Johguchi[2], Ken Takeuchi[2]
[1]Chuo Univ./Univ. of Tokyo, [2]Chuo Univ.

2:30PM
5A.4
A Compact Realization of a Quantum n-Bit Square Root Circuit
Nusrat Jahan lisa[1] and Hafiz Md. Hasan Babu[2]
[1]Ahsanullah University of Science and Technology, Dhaka, Bangladesh, [2]University of Dhaka, Bangladesh

2:50PM
5A.5
Statistical Process Variation Analysis of a Graphene FET based LC-VCO for WLAN Applications
Abir Khan, Saraju Mohanty, Elias Kougianos
University of North Texas, Denton

3:10PM
5A.6
An Efficient Semi-Analytical Current Source Model for FinFET Devices in Near/Sub-Threshold Regime Considering Multiple Input Switching and Stack Effect
Tiansong Cui, Shuang Chen, Yanzhi Wang, Shahin Nazarian, Massoud Pedram
University of Southern California

SESSION 5B

Wednesday March 5, 2014

Great America Meeting Room 2

Assertion and Formal Verification Technologies

Chair: **Srivatsa Vasudevan**, Synopsys
Co-Chair: **Abhilash Goyal**, Oracle

1:30PM
5B.1
Assertion-Based Verification for System-Level Designs
Hassan Sohofi and Zainalabedin Navabi
University of Tehran

1:50PM
5B.2
Coverage of Compositional Property Sets under Reactive Constraints
Binghao Bao[1], Jörg Bormann[2], Markus Wedler[1], Dominik Stoffel[1], Wolfgang Kunz[1]
[1]University of Kaiserslautern, [2]

2:10PM
5B.3
Automated Methods for Eliminating X Bugs
Kai-hui Chang, Yen-ting Liu, Chris Browy
Avery Design Systems

2:30PM
5B.4
Specification and Formal Verification of Power Gating in Processors
Amir Masoud Gharehbaghi and Masahiro Fujita
The University of Tokyo

2:50PM
5B.5
Formal Verification of Safety of Polymorphic Heterogeneous Multi-Core Architectures
Miroslav Velev and Ping Gao
Aries Design Automation

3:10PM
5B.6
Simulation and Satisfiability Guided Counter-example Triage for RTL Design Debugging
Zissis Poulos[1], Yu-Shen Yang[2], Andreas Veneris[1], Bao Le[1]
[1]University Of Toronto, [2]Advanced Micro Devices, Inc

SESSION 5C

Wednesday March 5, 2014

Great America Meeting Room 3

Thermal and Energy Considerations in Systems

Chair: **Hai Li**, University of Pittsburg
Co-Chair: **Duo Liu**, Chongqing University

1:30PM
5C.1
FastSpot: Host-Compiled Thermal Estimation For Early Design Space Exploration
Darshan Gandhi, Andreas Gerstlauer, Lizy John
The University of Texas at Austin

1:50PM
5C.2
Maximizing Throughput of Power/Thermal-Constrained Processors by Balancing Power Consumption of Cores
Abhishek Sinkar, Hao Wang, Nam Sung Kim
University of Wisconsin-Madison

2:10PM
5C.3
Building Energy-Efficient Multi-Level Cell STT-MRAM Based Cache Through Dynamic Data-Resistance Encoding
Ping Chi[1], Cong Xu[1], Xiaochun Zhu[2], Yuan Xie[1]
[1]Pennsylvania State University, [2]Qualcomm Incorporated

2:30PM
5C.4
Thermal Hotspot Reduction in mm-Wave Wireless NoC Architectures
Jacob Murray, Paul Wettin, Ryan Kim, Xinmin Yu, Partha Pande, Behrooz Shirazi, Deukhyoun Heo
Washington State University

2:50PM
5C.5
Energy-Aware Scratch-Pad Memory Partitioning for Embedded Systems
Florin Balasa[1], Noha Abuaesh[1], Cristian V. Gingu[2], Ilie I. Luican[3], Doru V. Nasui[4]
[1]American University in Cairo, [2]Fermilab, [3]Microsoft, Inc., [4]American International Radio, Inc.

3:10PM
5C.6
Energy Efficient Job Scheduling in Single-ISA Heterogeneous Chip-Multiprocessors
Ying Zhang[1], Lide Duan[2], Bin Li[1], Lu Peng[1], Srinivasan Sadagopan[2]
[1]Louisiana State University, [2]AMD Corporation

SESSION 6A

Wednesday March 5, 2014

Great America Meeting Room 1

Advanced Circuit and System Methodologies

Chair: **Charles Augstine**, Intel
Co-Chair: **Saibal Mukhopadhyay**, Georgia Tech

3:50PM
6A.1
ULSNAP: An Ultra-low Power Event-Driven Microcontroller for Sensor Network Nodes
Carlos Tadeo Ortega Otero, Jonathan Tse, Robert Karmazin, Benjamin Hill, Rajit Manohar
Cornell University

4:10PM
6A.2
An Energy-Efficient Mobile PAM Memory Interface for Future 3D Stacked Mobile DRAMs
Majid Jalalifar and Gyung-Su Byun
West Virginia University, Morgantown, WV USA

4:30PM
6A.3
Rapid Prototype and Implementation of a High-Throughput and Flexible FFT ASIP Based on LISA 2.0
Ting Chen[1], Xiaowei Pan[2], Hengzhu Liu[1], Tiebin Wu[1]
[1]school of Computer, National University of Defense Technology, [2]Aachen University of Technology

4:50PM
6A.4
A Spread Spectrum Clock Generator for Higher Modulatation Rate
GAUTAM KUMAR SINGH
ON Semiconductor

5:10PM
6A.5
Tradeoffs Between RTO and RTZ in WCHB QDI Asynchronous Design
Matheus Moreira[1], Julian Pontes[2], Ney Calazans[1]
[1]PUCRS-FACIN, [2]CEA-LETI

SESSION 6B

Wednesday March 5, 2014

Great America Meeting Room 2

Power Grid Analysis and Issues

Chair: **Rajan Beera**, Pall Corporation
Co-Chair: **Kamesh Gadepally**, Texas Instruments

3:50PM
6B.1
Statistical Analysis of Process Variation Induced SRAM Electromigration Degradation
Zhong Guan[1], Malgorzata Marek-Sadowska[1], Sani Nassif[2]
[1]ECE Department, University of California, Santa Barbara, [2]Austin Research Laboratory, IBM

4:10PM
6B.2
Estimating True Worst Currents for Power Grid Electromigration Analysis
Di-an Li and Malgorzata Marek-Sadowska
UCSB

4:30PM
6B.3
An Enlarged-Partition Based Preconditioned Iterative Solver for Parallel Power Grid Simulation
Le Zhang and Vivek Sarin
Texas A&M University

4:50PM
6B.4
A 3-D Fast Transform-Based Preconditioner for Large-Scale Power Grid Analysis on Massively Parallel Architectures
Konstantis Daloukas, Nestor Evmorfopoulos, Panagiota Tsompanopoulou, George Stamoulis
Department of Electrical and Computer Engineering, University of Thessaly

5:10PM
6B.5
On Pattern Generation for Maximizing IR Drop
Arunkumar Vijayakumar[1], Vinay C Patil[1], Girish Paladugu[2], Sandip Kundu[1]
[1]Electrical and Computer Engineering, University of Massachusetts , Amherst , USA, [2]Advanced Micro Devices , Boxborough , USA

SESSION 6C

Wednesday March 5, 2014

Great America Meeting Room 3

Smart Sensors Design Technology

Chair: **Daniela De Venuto**, Polytechnic of Bari, Italy
Co-Chair: **Phil Mather**, Maxim

3:50PM
6C.1
Design of a CMOS Readout Circuit for Wide-Temperature Range Capacitive MEMS Sensors
Yucai Wang and Vamsy Chodavarapu
McGill University

4:10PM
6C.2
Topology Optimization of a Passive Thermal Actuator
Harald Steiner[1], Wilfried Hortschitz[1], Franz Keplinger[2], Thilo Sauter[1]
[1]Center for Integrated Sensorsystems, Danube University Krems, [2]Institute of Sensor and Actuator Systems, Vienna University of Technology

4:30PM
6C.3
Thermal Flow Sensors based on Printed Circuit Board Technology
Thilo Sauter, Thomas Glatzl, Franz Kohl, Harald Steiner, Almir Talic
Danube University Krems

4:50PM
6C.4
Realization of Efficient RF Energy Harvesting Circuits Employing Different Matching Techniques
Sachin Agrawal, Sunil Kumar Pandey, Jawar Singh, Manoj Singh Parihar
PDPM IIITDM Jabalpur

5:10PM
6C.5
An Integrated Precision Clock Generator for Implanted Electronics with Superior Long-term Stability
Jiyuan Luan and Michael DiVita
Texas Instrument