WELCOME TO ISQED 2015

On behalf of the ISQED 2015 conference and technical committees, we are pleased to welcome you to the 16th International Symposium on Quality Electronic Design, ISQED 2015. The 16th International Symposium on Quality Electronic Design (ISQED 2015) is the premier interdisciplinary and multidisciplinary Electronic Design conference—bridges the gap among Electronic/Semiconductor ecosystem members providing electronic design tools, integrated circuit technologies, semiconductor technology, packaging, assembly & test to achieve design quality. ISQED is held with the technical sponsorship of IEEE CASS, IEEE EDS, and IEEE Reliability Society.

ISQED continues to provide and foster a unique opportunity to participants to interact and engage themselves in cutting edge tutorials, presentations, and panel and plenary sessions. We are happy to report a number of initiatives this year. The conference is organized around the theme 'IoT, Smart Sensors and Security'. And we have invited 4 distinguished keynote speakers from industry to focus on these topics.

Additionally six tutorials provide a holistic approach, from devices to circuits to systems, while covering in-depth studies and state-of-the-art in each of the topics impacting the quality of electronic design. The two-day technical program with three parallel sessions pack over 100 papers highlighting the latest trends in electronic circuit and system design & automation, test, verifications, and semiconductor technologies. A new track on Hardware Security is formed to bring forth the technical innovations and trends in electronic design in this important field. ISQED 2015 also features a panel discussion titled "Industry Panel on Hardware and System Security" on Tuesday March 3rd.

All the technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 2-4 at the Santa Clara Convention Center in Santa Clara, CA. Please refer to the conference booklet and/or ISQED website for program details.
We would like to thank the ISQED 2015 corporate sponsors: IBM, Synopsys, Innovotek, and Silicon Valley Polytechnic Institute for their valuable support of this conference. Welcome to another stellar year of ISQED! It couldn't have happened without your support and participation.

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Paul Wesling
Publication Chair

Bao Liu
Plenary Chair

Ali A. Iranmanesh
Founder & President

ISQED 2015 Best Paper Candidates

1A.1

Stack Based Sense Amplifier Designs for Reducing Input-Referred Offset

James Boley and Benton Calhoun

University of Virginia

1B.1

Thermal Sensor Allocation for SoCs Based on Temperature Gradients

Jun Yong Shin, Fadi Kurdahi, Nikil Dutt

University of California Irvine

1C.2

Electrical Characteristic and Power Consumption Fluctuations of Trapezoidal Bulk FinFET Devices and Circuits Induced by Random Line Edge Roughness

SChieh-Yang Chen, Wen-Tsung Huang, and Yiming Li

National Chiao Tung University, Taiwan

2C.2

Preemptive Built-In Self-Test for In-Field Structural Testing

Panagiotis Sismanoglou, Vlasis Pitsios and Dimitris Nikolos

University of Patras, Greece

6C.2

Technology/Circuit Co-optimization and benchmarking for Graphene Interconnects at Sub-10nm Technology Node

Chenyun Pan[1], Praveen Raghavan[2], Francky Catthoor[2], Zsolt Tokei2 and Azad Naeemi[1]

[1]Georgia Institute of Technology, [2]IMEC, Belgium

5C.4

Resource Allocation Methodology for Through Silicon Vias and Sleep Transistors in 3D ICs

Hailang Wang and Emre Salman

Stony Brook University, NY

5C.6

Novel Adaptive Power Gating Strategy of TSV-Based Multi-Layer 3D IC

Seungwon Kim, Seokhyung Kang, Ki Jin Han, and Youngmin Kim

Ulsan National Institute of Science and Technology (UNIST), Korea

6A.1

A Low-Power Field-Programmable Analog Array for Wireless Sensing

Brandon Rumberg and David W. Graham

West Virginia University, Morgantown

ISQED 2015 Best Papers

Best Papers

1C.2

Electrical Characteristic and Power Consumption Fluctuations of Trapezoidal Bulk FinFET Devices and Circuits Induced by Random Line Edge Roughness

SChieh-Yang Chen, Wen-Tsung Huang, and Yiming Li

National Chiao Tung University, Taiwan

6A.1

A Low-Power Field-Programmable Analog Array for Wireless Sensing

Brandon Rumberg and David W. Graham

West Virginia University, Morgantown

* Authors of best papers are honored during the luncheon on Tuesday March 3

ISQED 2015 FELLOW AWARD

MELY CHEN CHI
Chung Yuan Christian University, Taiwan

Mely Chen Chi received her BS in physics from National Taiwan Normal University and her PhD in physics from Wesleyan University. She has been worked in the research and development of Electronic Design Automation since 1978 when she joined Bell Laboratories. At 1990 she became manager of the Industrial Technology Research Institute in Hsinchu, Taiwan. She is in charge of the VLSI & System Design Automation in the Computer & Communication Industrial Research Institute.
She became a professor since 1999 and set up Electronics and Information Research and Development Center. She has educated and trained students to win many outstanding awards in the annual contests of VLSI Computer Aided Design Software Development in Taiwan. She was one of the founding member of the International Symposium on Quality Electronic Design and served as Global Representative Chair of Taiwan for 15 years. She is the author of more than 60 papers.

ISQED 2015 FELLOW AWARD

Syed M. Alam
Everspin Technologies, Inc.

Syed M. Alam received his PhD and MS in Electrical Engineering from MIT in 2004 and 2001, respectively, and BS in Electrical Engineering from UT Austin in 1999. He is currently the chip design lead for Spin Transfer Torque MRAM at Everspin Technologies, Inc. In addition to project management and technical leadership, he is hands-on with custom circuit design of mixed-signal memory circuits including array, senseamps, write drivers, datapath, ECC, DDR3 blocks and architecture. Dr. Alam has contributed to a portfolio of key STT-MRAM design, architecture, and test IP.

Dr. Alam has served on PhD thesis committees and mentored/co-advised five PhD students for research on through-Si via parasitic and noise modeling, power bus in 3D, and logic-in-memory architecture with nanomagnetic logic. Dr. Alam has developed new lecture notes on 3D integration and nonvolatile memories, and teaches graduate-level course lectures on nonvolatile memory at UT Austin. Dr. Alam has served on technical program committees of multiple conferences including ISQED, DAC, DATE, and ICCAD. He has been involved with ISQED for over 10 years and recently in leadership roles as General chair, TPC chair, and tutorial chair. He is a reviewer for IEEE TVLSI, TCAS, TCAD, and TED. Dr. Alam has over 65 publications in refereed journals and conferences, two book chapters, and over 45 patents issued or pending.

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Thilo Sauter - Danube University Krems

NOTES

ISQED 2015
GENERAL INFORMATION

March 2-4, 2015
Santa Clara Convention Center
5001 Great America Pkwy, Santa Clara, CA 95054

TUTORIALS

Monday Tutorials

Monday, March 2, 9:00am-4:30pm
Great America Meeting Room 3

Chair:
Arijit Raychowdhury - *Georgia Institute of Technology*

Co-Chair:
Hai (Helen) Li - *University of Pittsburgh*

The Frontiers of Robust Circuit Design in Sub-28nm Process Technologies

Jim Dodrill, *ARM*

Powering Microsystems

Prof. Gabriel A. Rincón-Mora - *Georgia Tech*

Reliability Challenges in Sub 20nm Technology

Dr. Tanya Nigam - *GLOBALFOUNDRIES*

Secure Hardware in the Nano Era: Some New Directions

Prof. Swarup Bhunia - *Case Western*

Security and Validation in SoC Designs - Cooperation, Conflicts, and Trade-offs

Dr. Sandip Ray - *Intel Corporation*

Neuromorphic Computing based Processors

Prof. Hao Jiang - *San Francisco State University*

KEYNOTE SPEECHES

Plenary Session 1P

Tuesday, March 3, 9:00am - 10:00am
Great America Ballroom

Rethinking Design Creation, Verification and Validation for the Internet of Things

George Zafiropoulos
Vice President of Solutions Marketing in the AWR Group
National Instruments

What's Really Driving the Internet of Things? – Insights on the Market, Technology and Challenges

Mike Ballard
Sr. Manager, Home Appliance Solutions and Smart Energy Groups
Microchip Technology

ISQED LUNCH & PANEL DISCUSSION

Tuesday, March 3, 12:00pm-1:30pm
Great America Ballroom

ISQED AWARDS CEREMONY

Tuesday, March 4, 12:00pm-12:30pm
Great America Ballroom

ISQED Best Paper Awards

Recipients of the ISQED 2015 Best Paper Award will be recognized during the ISQED luncheon on Tuesday. List of best papers is shown in Page 2 of this document.

12:30pm-1:30pm

Luncheon Panel Discussion

Industry Panel on Hardware and System Security

Panelists:
ARM, Intel, Microsemi, Cadence, Freescale

GENERAL INFORMATION

KEYNOTE SPEECHES

Plenary Session 2P

Wednesday, March 4, 9:00am - 10:00am
Great America Ballroom

From Cluster to Cloud:
How to Harness the Internet of Things

Jay Muelhoefer
Director of Software Defined Portfolio Marketing
IBM

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Connecting the Dots to achieve high Reliability and Quality

Raj N. Master
General Manager, Reliability, Quality and Silicon Operations
Microsoft

TECHNICAL SESSIONS

There are a total of 18 technical sessions held on Tuesday and Wednesday. Technical sessions are held in the format of 3 parallel tracks in **Great America Meeting Rooms 1-3**.

Poster Papers & Mixer

Poster display will take place on Tuesday afternoon 5:30pm-7:00pm in the Atrium area outside of **Great America Meeting Rooms 1-3**. Authors will be available to discuss their works and to answer questions. Refreshments will be served.

ON-SITE REGISTRATION

Tentative time schedule of on-site registration is as follows:

Monday, March 2	*7:30am-4:00pm*
Tuesday, March 3	*8:00am-5:00pm*
Wednesday, March 4	*8:00am-1:00pm*

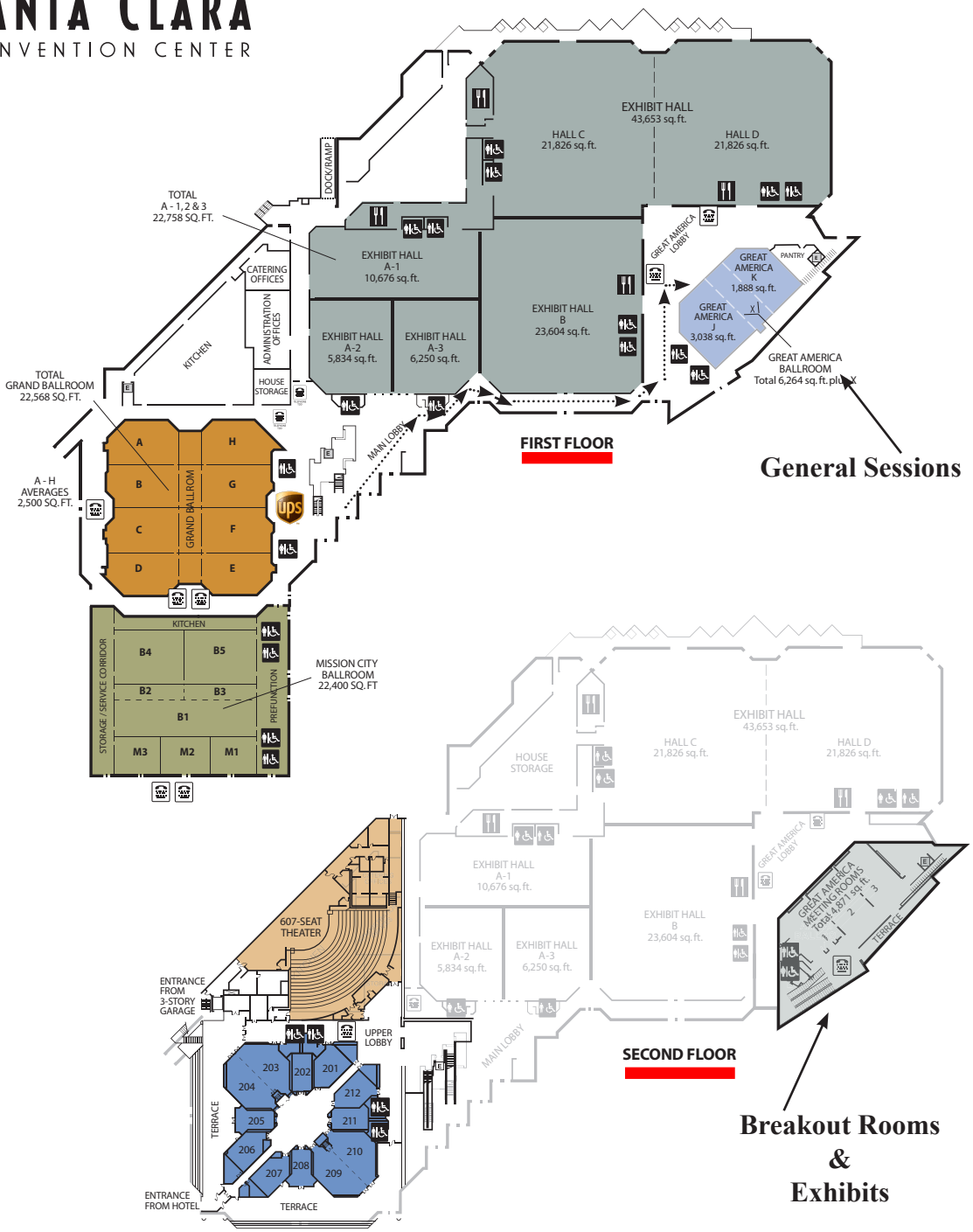
Registration desk location will be alternate between the location beside Great America meeting rooms 1-3, and the location beside Great America Ballroom.

Co-located Events

IoT Summit
March 5-6
Great America Meeting Room 2
www.IoT-Summit.org

FLOOR PLAN

SANTA CLARA
CONVENTION CENTER



PROGRAM AT A GLANCE

ISQED 2015 PROGRAM AT A GLANCE

DATE	TIME			
MONDAY 3/2/2015	*9:00AM-4:30PM*	**TUTORIALS** **GREAT AMERICA MEETING ROOM 3** **THE FRONTIERS OF ROBUST CIRCUIT DESIGN IN SUB-28NM PROCESS TECHNOLOGIES** **JIM DODRILL** - *ARM* **POWERING MICROSYSTEMS** **PROF. GABRIEL A. RINCÓN-MORA** - *GEORGIA TECH* **RELIABILITY CHALLENGES IN SUB 20NM TECHNOLOGY** **DR. TANYA NIGAM** - *GLOBALFOUNDRIES* **SECURE HARDWARE IN THE NANO ERA: SOME NEW DIRECTIONS** **PROF. SWARUP BHUNIA** - *CASE WESTERN* **SECURITY AND VALIDATION IN SOC DESIGNS - COOPERATION, CONFLICTS, AND TRADE-OFFS** **DR. SANDIP RAY** - *INTEL CORPORATION* **NEUROMORPHIC COMPUTING BASED PROCESSORS** **PROF. HAO JIANG** - *SAN FRANCISCO STATE UNIVERSITY*		
TUESDAY 3/3/2015	*9:00AM-10:00AM*	**PLENARY SESSION 1P** **(GREAT AMERICA BALLROOM)** **KEYNOTE SPEECHES BY:** **GEORGE ZAFIROPOULOS** - *NATIONAL INSTRUMENTS*, **MIKE BALLARD** - *MICROCHIP TECHNOLOGY*		
	10:00AM-10:20AM	**MORNING BREAK**		
	10:20AM-12:00PM	**SESSION 1A** **ROBUST MEMORY DESIGN** **GREAT AMERICA MEETING ROOM 1**	**SESSION 1B** **ADVANCES IN PHYSICAL DESIGN & OPTIMIZATION** **GREAT AMERICA MEETING ROOM 2**	**SESSION 1C** **MANUFACTURING, MODELING, AND DESIGN ISSUES IN NANOSCALE CMOS** **GREAT AMERICA MEETING ROOM 3**
	12:00PM-12:45PM	**ISQED PANEL & LUNCHEON** **(GREAT AMERICA BALLROOM)** **BEST PAPER AWARDS , COMMITTEE RECOGNITION AWARDS** **LUNCHEON PANEL DISCUSSION** **INDUSTRY PANEL ON HARDWARE AND SYSTEM SECURITY** ARM, INTEL, MICROSEMI, CADENCE, FREESCALE		
	1:30PM-3:30PM	**SESSION 2A** **VOLTAGE REGULATORS AND ANALOG DESIGN** **GREAT AMERICA MEETING ROOM 1**	**SESSION 2B** **ARCHITECTURAL ANALYSIS AND ALGORITHMS** **GREAT AMERICA MEETING ROOM 2**	**SESSION 2C** **BIST AND SCAN TESTING** **GREAT AMERICA MEETING ROOM 3**
	3:30PM-3:50PM	**AFTERNOON BREAK**		
	3:50PM-5:30PM	**SESSION 3A** **LOW POWER CIRCUIT DESIGN** **GREAT AMERICA MEETING ROOM 1**	**SESSION 3B** **ENERGY AND POWER MANAGEMENT FOR IOT** **GREAT AMERICA MEETING ROOM 2**	**SESSION 3C** **LOW-POWER AND ROBUST DESIGN TECHNIQUES** **GREAT AMERICA MEETING ROOM 3**
	5:30PM-7:00PM	**POSTER PAPERS & MIXER** **HALLWAY OUTSIDE GREAT AMERICA MEETINGS ROOMS**		
WEDNESDAY 3/4/2015	*9:00AM-10:00AM*	**PLENARY SESSION 2P** **(GREAT AMERICA BALLROOM)** **KEYNOTE SPEECHES BY:** **JAY MUELHOEFER** - *IBM*, **RAJ N. MASTER** - *MICROSOFT*		
	10:00AM-10:20AM	**MORNING BREAK**		
	10:20AM-12:00PM	**SESSION 4A** **CHALLENGES IN SOC DESIGN** **GREAT AMERICA MEETING ROOM 1**	**SESSION 4B** **NETWORK AND MULTIPROCESSING SYSTEMS** **GREAT AMERICA MEETING ROOM 2**	**SESSION 4C** **VERIFICATION AND DELAY MEASUREMENT** **GREAT AMERICA MEETING ROOM 3**
	12:00PM-1:00PM	**NETWORKING LUNCH**		
	1:00PM-3:00PM	**SESSION 5A** **HARDWARE AND SYSTEM SECURITY** **GREAT AMERICA MEETING ROOM 1**	**SESSION 5B** **SYSTEMS IMPLEMENTATION AND OPTIMIZATION** **GREAT AMERICA MEETING ROOM 2**	**SESSION 5C** **PACKAGING AND 3D INTEGRATION** **GREAT AMERICA MEETING ROOM 3**
	3:00PM-3:20PM	**AFTERNOON BREAK**		
	3:20PM-5:00PM	**SESSION 6A** **SENSOR TECHNOLOGY** **GREAT AMERICA MEETING ROOM 1**	**SESSION 6B** **EDA FOR DESIGN EXPLORATION & ANALYSIS BEYOND MOORE'S LAW** **GREAT AMERICA MEETING ROOM 2**	**SESSION 6C** **EMERGING SOLID-STATE DEVICE AND INTERCONNECT TECHNOLOGIES** **GREAT AMERICA MEETING ROOM 3**

Tuesday March 3

9:00am-9:30am
Great America Ball Rooms

Rethinking Design Creation, Verification and Validation for the Internet of Things

George Zafiropoulos
National Instruments

The proliferation of IoT devices is driving the design process to produce ever smaller, lower cost, and more highly integrated systems, with shorter time to market. To meet these challenges, we need to streamline the process of design and test and look for opportunities to become much more efficient. New methodolodies we be necessary to improve the design to test flow, system validation and improve test IP re-use. In this presentation we will explore some ideas of how to improve the overall design and test process.

About George Zafiropoulos

George Zafiropoulos is Vice President of Solutions Marketing in the AWR Group of National Instruments. George has spent over 30 years in semiconductor design automation engineering, marketing, and executive management roles at Quickturn, Synopsys, and Cadence. In his role at National Instruments, George is looking at methods to improve the overall design to test process including analog, digital, RF and embedded software. George is also on the board of Ladera Labs and TeleSense, two IoT startups in Silicon Valley.

Tuesday March 3

9:30am-10:00am
Great America Ball Rooms

What's Really Driving the Internet of Things? – Insights on the Market, Technology and Challenges

Mike Ballard
Microchip Technology

The Internet of Things is an embryonic market that is currently driving a great deal of interest within the semiconductor industry. Not only as a compelling and potentially huge market that will create new sources of revenue for years to come, but also as a platform for technology innovations. But what is really behind this interest? What benefits could be derived from adding technology to many everyday products? What challenges do designers face when architecting these innovative systems? This keynote will answer these questions while providing a high-level overview of the market and insight into its differing communication standards. It will also discuss the challenges that extend beyond the embedded product, such as security and connecting to the cloud.

About Mike Ballard

Michael Ballard received his Bachelor's of Science in Electrical Engineering from Ohio University's Russ College of Engineering and Technology. He began his career in the power-generation market and then migrated over to automotive electronics, where he spent 10 years with automotive OEMs and semiconductor providers. In 2007, Michael transitioned into the appliance market as the Manager of Microchip's Home Appliance Solutions Group. In 2010, in addition to his Home Appliance responsibilities, Michael was charged with running the newly-created Smart Energy Group. In 2012, due to his group's knowledge and leadership in the emerging market, he also created a new team at Microchip focused on the Internet of Things. Michael has also been the leader of Microchip's Marketing Council for the past two years. He has been an industry leader in the Smart-Energy, IoT, and Appliance markets, and has written many papers and articles. Additionally, Michael sits on a number of task forces and advisory panels associated with these industries, including serving as a member of the Boards of Directors for the Association of Home Appliance Manufacturers (AHAM) and USNAP.

Wednesday March 4

9:00am-9:30am
Great America Ball Rooms

From Cluster to Cloud: How to Harness the Internet of Things

Jay Muelhoefer
IBM

The Internet of Things and smart sensors are generating ever increasing amounts of data. Organizations are using public and private clouds to transfer and process this data, but bringing along challenges such as data duplication, under utilized disk storage and idle CPUs, with little or no prioritization. New developments in data aware scheduling will be described. These work with IBM Platform Computing workload management tools and intelligent caching to schedule and deliver data using the cloud. Combined with powerful solutions, this talk will highlight how organizations take advantage of intelligent data scheduling, enhanced workload management and efficient compute utilization, including case studies and client examples. Further the talk will showcase how all of these technologies are making cloud computing less expensive and more secured.

About Jay Muelhoefer

Jay Muelhoefer is the Director of Software Defined Portfolio Marketing in the Systems and Technology Group of IBM. His role spans software defined infrastructure offerings for big data and Hadoop, high performance computing (HPC), analytics, cloud, and software defined storage for both on-premise and cloud environments. Jay has been CMO and General Manager of technology companies ranging from database monitoring, SaaS, and PLM and was a strategy consultant for Booz Allen & Hamilton. Jay holds an MBA from Harvard Business School and a Masters and Bachelors in Engineering from the Massachusetts Institute of Technology.

Wednesday March 4

9:30am-10:00am
Great America Ball Rooms

Connecting the Dots to achieve high Reliability and Quality

Raj N. Master
Microsoft

The ubiquitous trend towards a connected, digital, always-ON lifestyle is driving the development of electronic devices that have smaller form factors, higher performance requirements, along with expectations of reliability and quality. Consumers don't buy products because of high quality but expect it. The result is a constant upward pressure on delivering high reliability at silicon, package and system level. Although this general trend holds for applications in the computing arena, gaming console arena, consumer electronics arena as well as in the portable electronics arena, the relative constraints on the cost, size and complexity of the products make this a challenging task. This is further made more difficult by unpredictable ways consumers may use the product. Microsoft evolution of hardware and reliability challenges of Surface will be described to achieve a highly reliable and quality product.

About Raj N. Master

Raj joined Microsoft in 2008. He is General Manager for IC Packaging, Silicon Operations, Quality and Reliability for all hardware products in Microsoft. These include Xbox, Kinect, Surface, Accessories, Zune, Keyboard, Mouse ,Webcam, and Roundtable etc. Raj was Corporate Fellow and Chief Technologistist for AMD from 1996 -2008. He was responsible to successfully transfer the IBM C4 / BGA technologies to AMD and set up high volume manufacturing in Penang which has to date produced more then 400 million flip chip assemblies. He led the Organic packaging development and manufacturing which is now in high volume production. He was also responsible to build, qualify and provide technical direction to AMD Flip Chip Bumping and probing operations in Dresden, Germany. He provides technical guidance for equipment and processes for C4 /BGA manufacturing lines in Suzhou, Penang and Singapore. He also provided technical expertise and guidance to product lines, Failure analysis, and reliability and quality organizations within AMD. He was also manager of the Lead Free program of AMD working with US companies, Chinese Governments and EU to align the Lead Free exemptions. Raj joined AMD after spending 21 years at IBM. He was Senior Technical Staff member at IBM prior to joining AMD. He was responsible for packaging development and manufacturing as related to C4, Ball Grid Array, Column Grid Array, Board Level Reliability and Multi Layer Ceramic Substrate. . Raj has 51 U.S. patents issued to him and has published over 80 technical papers. Raj was given IEEE " Electronics Manufacturing Technology Award" For pioneering managerial and technical leadership in packaging technology and manufacturing, thermal solutions, substrate technology and manufacturing, and flip chip bumping that significantly impacted advancements of electronic products in the industry in May 2014.

SESSION 1A

Tuesday March 3, 2015

Robust Memory Design

Chair: **Kurt Schwartz**, Texas Instruments
Co-Chair: **Charles Augustine**, Intel

10:20AM
1A.1
Stack Based Sense Amplifier Designs for Reducing Input-Referred Offset
James Boley and Benton Calhoun
University of Virginia

10:40AM
1A.2
Designing Low-VTH STT-RAM for Write Energy Reduction in Scaled Technologies
Farah Yahya[1], Mohammad Mansour[2], James Tschanz[3], Muhammad Khellah[3]
[1]University of Virginia, Charlottesville VA, [2]American University of Beirut, Lebanon, [3]Intel Corp.

11:00AM
1A.3
High Performance and High Yield 5 nm Underlapped FinFET SRAM Design Using P type Access Transistors
Roohollah Yarmand[1], Behzad Ebrahimi[1], Hassan Afzali-Kusha[2], Ali Afzali-Kusha[1], Massoud Pedram[2]
[1]University of Tehran, [2]University of Southern California

11:20AM
1A.4
Stability Analysis of Single-Ended Boost-Less Sub-threshold 7T FinFET SRAM Cell under Process-Voltage-Temperature Variations
Chandrabhan Kushwah[1], Santosh Kumar Vishvakarma[1], Devesh Dwivedi[2]
[1]IIT Indore, [2]IBM Bangalore

11:40AM
1A.5
An Energy-Efficient On-Chip Memory Structure for Variability-Aware Near-Threshold Operation
Jun Shiomi, Tohru Ishihara, Hidetoshi Onodera
Kyoto University

SESSION 1B

Tuesday March 3, 2015

Advances in Physical Design & Optimization

Chair: **Srini Krishnamoorthy**, AMD
Co-Chair: **Vamsi Srikantam**, Applied Micro

10:20AM
1B.1
Thermal Sensor Allocation for SoCs Based on Temperature Gradients
Jun Yong Shin, Fadi Kurdahi, Nikil Dutt
University of California Irvine

10:40AM
1B.2
Clock Skew Optimization for Maximizing Time Margin by Utilizing Flexible Flip-Flop Timing
Hyungjung Seo, Jeongwoo Heo, Taewhan Kim
Seoul National University

11:00AM
1B.3
Large-scale Multi-corner Leakage Optimization Under the Sign-off Timing Environment
George Gonzalez, Murari Mani, Mahesh Sharma
AMD

11:20AM
1B.4
Fast Obstacle-Avoiding Octilinear Steiner Minimal Tree Construction Algorithm for VLSI Design
Xing Huang, Wenzhong Guo, Guolong Chen
Fuzhou university

11:40AM
1B.5
A Router for Via Configurable Structured ASIC with Standard Cells and Relocatable IPs
Chiung-Chih Ho, Hsin-Pei Tsai, Liang-Chi Lai, Rung-Bin Lin
Yuan Ze University

SESSION 1C

Tuesday March 3, 2015

Manufacturing, Modeling, and Design Issues in Nanoscale CMOS

Chair: **Rajan Beera**, Pall Corporation
Co-Chair: **Vivek Joshi**, GLOBALFOUNDRIES

10:20AM
1C.1
Circuit Design Perspectives for Ge FinFET at 10nm and Beyond
S. Sinha[1], L. Shifren[2], V. Chandra[2], B. Cline[1], G. Yeric[1], R. Aitken[2], B. Cheng[3], A. R. Brown[3], C. Riddet[3], C. Alexander[3], C. Millar[3], A. Asenov[3]
[1]ARM Inc., Austin, TX, [2]ARM Inc., San Jose, CA, [3]Gold Standard Simulations Ltd., Glasgow, Scotland

10:40AM
1C.2
Electrical Characteristic and Power Consumption Fluctuations of Trapezoidal Bulk FinFET Devices and Circuits Induced by Random Line Edge Roughness
Chieh-Yang Chen, Wen-Tsung Huang, Yiming Li
National Chiao Tung University

11:20AM
1C.4
GlYFF: A Framework for Global Yield and Floorplan Aware Design Optimization
Shuo Wang, Yue Gao, Melvin Breuer
University of Southern Caifornia

11:40AM
1C.5
Method for Efficient Flash Bit Cell Current Compression in Deeply Erased Bits
Jon Nafziger and Dan Burggraf
Texas Instruments

SESSION 2A

Tuesday March 3, 2015

Voltage Regulators and Analog Design

Chair: **Aswin Mehta**, Texas Instruments
Co-Chair: **Charles Augustine**, Intel

1:30PM
2A.1
A Simplified Single-Inductor Dual-Output DC-DC Buck Converter Architecture with a Fully Digital Σ−Δ Based Controller
Nijad Anabtawi[1] and Rony Ferzli[2]
[1]Intel Corporation, [2]Arizona State University

1:50PM
2A.2
A CMOS Hysteretic DC-DC Buck Converter with a Low Output Ripple Voltage
Tae Jin Chung and Kwang Yoon
Inha University

2:10PM
2A.3
A 4-14 Gbps Inductor-Less Adaptive Linear Equalizer in 65nm CMOS Technology
Govardhana Rao Talluri, Rakesh K K, Maryam Shojaei Baghini
IIT Bombay

2:30PM
2A.4
A Digitally-Controlled Power-Aware Low-Dropout Regulator to Reduce Standby Current Drain in Ultra-Low-Power MCU
Kaushik Mazumdar[1], Steven Bartling[2], Sudhanshu Khanna[2], Mircea Stan[1]
[1]University of Virginia, [2]Texas Instruments

2:50PM
2A.5
A Radiation-Hardened-By-Design Phase-Locked Loop Using Feedback Voltage Controlled Oscillator
Seok Min Jung and Janet Roveda
University of Arizona

3:10PM
2A.6
Design of a Sigma-Delta Modulator in Standard CMOS Process for Wide-Temperature Applications
Yucai Wang and Vamsy Chodavarapu
McGill University

SESSION 2B

Tuesday March 3, 2015

Architectural Analysis and Algorithms

Chair: **Vivek Nandakumar**, Synopsys, Inc.
Co-Chair: **Hai (Helen) Li**, University of Pittsburgh

1:30PM
2B.1
Architectural Reliability Estimation using Design Diversity
Zheng Wang[1], Liu Yang[1], Anupam Chattopadhyay[2]
[1]RWTH-Aachen University, [2]Nanyang Technological University

1:50PM
2B.2
Tabu Search Based Multiple Voltage Scheduling under both Timing and Resource Constraints
Jianmo Ni, Nan Wang, Takeshi Yoshimura
Waseda University

2:10PM
2B.3
Cache-Aware SPM Allocation Algorithms for Hybrid SPM-Cache Architectures
Lan Wu and Wei Zhang
Virginia Commonwealth University

2:30PM
2B.4
Task Partitioning Optimization Algorithm for Energy Saving and Load Balance on NoC-based MPSoCs
Marco Stefani, Thais Webber, Ramon Fernandes, Rodrigo Cataldo, Letícia Poehls, César Marcon
PUCRS

2:50PM
2B.5
Improved Pipeline data Flow for DySER-based Platform
Zijian Hou[1], Xin Chen[2], Weifeng He[1]
[1]Shanghai Jiao Tong University, [2]Tongji University

3:10PM
2B.6
Rapid Heterogeneous Prototyping From Simulink
Shen Feng, Chris Driscoll, Jerediah Fevold, Hao Jiang, Gunar Schirner
ECE, Northeastern University

SESSION 2C

Tuesday March 3, 2015

BIST and Scan Testing

Chair: **Miroslav Velev**, Aries Design Automation
Co-Chair: **Jon Nafziger**, Texas Instruments

1:30PM
2C.1
Deterministic-Aware Pattern Transformation for Improving LBIST Pattern Quality
Gustavo Contreras[1], *Mark Tehranipoor*[1], *Nisar Ahmed*[2], *LeRoy Winember*[2], *Yang Zhao*[1]
[1]University of Connecticut, [2]Freescale Semiconductor Inc.

1:50PM
2C.2
Preemptive Built-In Self-Test for In-Field Structural Testing
Panagiotis Sismanoglou, Vlasis Pitsios, Dimitris Nikolos
University of Patras

2:10PM
2C.3
A Scan Shifting Method based on Clock Gating of Multiple Groups for Low Power Scan Testing
Sungyoul Seo[1], *Yong Lee*[1], *Joohwan Lee*[2], *Sungho Kang*[1]
[1]Department of Electronic Engineering, Yonsei University, Seoul, Korea, [2]Samsung Electronics, Korea

2:30PM
2C.4
Designing Effective Scan Compression Solutions for Industrial Circuits
Subramanian Chebiyam, Anshuman Chandra, Rohit Kapur
Synopsys Inc

2:50PM
2C.5
Low Power Scan Bypass Technique with Test Data Reduction
Hyunyul Lim, Wooheon Kang, Sungyoul Seo, Yong Lee, Sungho Kang
Department of Electrical and Electronic Engineering Yonsei University, Seoul, Korea

3:10PM
2C.6
Incremental ATPG methods for multiple faults under multiple fault models
Masahiro Fujita[1], *Alan Mishchenko*[2], *Naoki Taguchi*[1], *Kentaro Iwata*[1]
[1]University of Tokyo, [2]University of California, Berkeley

SESSION 3A

Tuesday March 3, 2015

Low Power Circuit Design

Chair: **Rangharajan Venkatesan**, Texas Instruments
Co-Chair: **Charles Augustine**, Intel

3:50PM
3A.1
Energy Reduction by Built-in Body Biasing with Single Supply Voltage Operation
Norihiro Kamae, A.K.M. Mahfuzul Islam, Akira Tsuchiya, Tohru Ishihara, Hidetoshi Onodera
Kyoto University

4:10PM
3A.2
Design of an Incoherent IR-UWB Receiver Front-End in 180-nm CMOS Technology
Jihai Duan, Qiangyu Hao, Yu Zheng, Baolin Wei, Weilin Xu
School of Information & Communication,Guilin University of Electronic Technology, Guilin, China

4:30PM
3A.3
Analysis and Optimization of Flip-Flops Under Process and Runtime Variations
Mohammad Saber Golanbari[1], Saman Kiamehr[1], Mehdi B. Tahoori[1], Sani Nassif[2]
[1]Karlsruhe Institute of Technology, [2]Radyalis LLC

4:50PM
3A.4
Energy Efficient Design of DVB-T2 Constellation Demapper
Nourhan Bahgat, DiaaEldin Khalil, Salwa El-Ramly
ECE Department, Ain Shams University, Cairo, Egypt

5:10PM
3A.5
Advanced Encryption System with Dynamic Pipeline Reconfiguration for Minimum Energy Operation
Srivatsan Chellappa, Chandarasekaran Ramamurthy, Vinay Vashishtha, Lawrence Clark
Arizona State University

SESSION 3B

Tuesday March 3, 2015

Energy and Power Management for IOT

Chair: **Hai (Helen) Li**, University of Pittsburgh
Co-Chair: **Lei Wang**, University of Connecticut

3:50PM
3B.1
Temperature Aware Refresh for DRAM Performance Improvement in 3D ICs
Menglong Guan and Lei Wang
Department of Electrical and Computer Engineering University of Connecticut

4:10PM
3B.2
Adaptive Tracking Channel Control for GNSS Receivers under Renewable Energy
Wenjie Huang and Lei Wang
University of Connecticut

4:30PM
3B.3
Novel SAT-based Invariant-Directed Low-Power Synthesis
Mahmoud Elbayoumi[1], *Michael Hsiao*[1], *Mustafa Elnainay*[2]
[1]Virginia Tech, [2]Alexanderia University

4:50PM
3B.4
Application and OS unconscious Power Manager for SoC Systems
Hend Affes, Amal Chaker, Michel Auguin
University Nice Sophia Antipolis

5:10PM
3B.5
Orchestrating Application Quality and Energy Storage Management in Solar-Powered Embedded Systems
Nga Dang, Hossein Tajik, Nikil Dutt, Nalini Venkatasubramanian, Eli Bozorgzadeh
University of California, Irvine

SESSION 3C

Tuesday March 3, 2015

Low-power and Robust Design Techniques

Chair: **Syed Alam**, Everspin
Co-Chair: **Saibal Mukhopadhyay**, Georgia Tech

3:50PM
3C.1
Optimal Choice of FinFET Devices for Energy Minimization in Deeply Scaled Technologies
Mohammad Saeed Abrishami, Alireza Shafaei Bejestan, Yanzhi Wang, Massoud Pedram
University of Southern California

4:10PM
3C.2
Ultra-Fast Variability-Aware Optimization of Mixed-Signal Designs using Bootstrapped Kriging
Saraju Mohanty, Elias Kougianos, Venkata Yanambaka
University of North Texas

4:30PM
3C.3
Novel Technique for P-hit Single-Event Transient Mitigation Using Enhance Dummy Transistor
Wang TianQi, Xiao LiYi, Huo MingXue, Qi ChunHua, Liu ShanShan
Harbin Institute of Technology

4:50PM
3C.4
Signal Domain Based Reachability Analysis in RTL Circuits
Sharad Bagri, Kelson Gent, Michael Hsiao
Virginia Tech

5:10PM
3C.5
Equivalence Checking of Scheduling in High-Level Synthesis
Tun Li, Jian Hu, Yang Guo, Sikun Li, Qingping Tan
NUDT

SESSION P

Tuesday March 3, 2015

Poster Session & Mixer

Chair: **Peter Wright**, Synopsys
Co-Chair: **Saibal Mukhopadhyay**, Georgia Institute of Technology

5:30PM
P.1
Design and Analysis of Low Pass Microstrip Filters using MATLAB
Luv Tomar[1], Saurabh Gupta[2], Raghuvir Tomar[3], Prakash Bhartia[4]
[1]Carleton University, [2]Neutrino IT Technologies, [3]The LNM Institute of Information Technology, [4]NATEL Engineering Co., Inc.

5:30PM
P.2
Employing Dynamic Body-Bias for Short Circuit Power Reduction in SRAMs
Yakup Murat mert[1] and Osman Seckin simsek[2]
[1]TUBİTAK İLTAREN, [2]ODTU

5:30PM
P.3
Accurate Standard Cell Characterization and Statistical Timing Analysis using Multivariate Adaptive Regression Splines
Taizhi Liu, Chang-Chih Chen, Linda Milor
Georgia Institute of Technology

5:30PM
P.4
Design Optimization of Sense Amplifiers using Deeply-scaled FinFET Devices
Alireza Shafaei Bejestan[1], Yanzhi Wang[1], Antonio Petraglia[2], Massoud Pedram[1]
[1]University of Southern California, [2]Federal University of Rio de Janeiro

5:30PM
P.5
A Fault Prediction Module for a Fault Tolerant NoC Operation
Jarbas Silveira[1], Mathieu Bodin[2], João Marcelo Ferreira[1], Thais Webber[3], César Marcon[4]
[1]LESC-DETI, [2]Polytechnique Nice-Sophia, [3]PPGEE/PUCRS, [4]PPGCC/PUCRS

5:30PM
P.6
User Power-Delay Budget Driven PSO Based Design Space Exploration of Optimal k-cycle Transient Fault Secured Datapath during High Level Synthesis
Anirban Sengupta and Saumya Bhadauria
Indian Institute of Technology, Indore

5:30PM
P.7
A Distinctive O(mn) Time Algorithm for Optimal Buffer Insertions
Xinsheng Wang[1], Wenpan Liu[1], Mingyan Yu[2]
[1]Harbin Institute of Technology, [2]Ningbo Institute of Technology Zhejiang University

5:30PM
P.8
Design and Analysis of Novel SRAM PUFs with Embedded Latch for Robustness
Jae-Won Jang and Swaroop Ghosh
University of South Florida

5:30PM
P.9
Fast Synthesis of Low Power Clock Trees Based on Register Clustering
Chao Deng, Yici Cai, Qiang Zhou
Tsinghua University

5:30PM
P.11
Irregular Shaped Voltage Islands Generation with Hazard and Heal Strategy
Zhen Meng, Song Chen, Lu Huang
Department of Electronic Science and Technology, USTC, China

5:30PM
P.12
Impact of Geometry Parameter on Electromigration Reliability in FCBGA Package
Lihua Liang[1], Yuanxiang Zhang[2], Richard Rao[3]
[1]Zhejiang University of Technology, [2]Quzhou University, [3]Vitesse Semiconductor Corporation

5:30PM
P.13
Enhancing System-Wide Power Integrity in 3D ICs with Power Gating
Hailang Wang and Emre Salman
Stony Brook University

5:30PM
P.14
Design of a Low-power UHF RFID Tag Baseband with Three-level Clock-gating Technique
Haibo Liao[1], Bin Wang[1], Weixin Kong[2], Yonghua Hu[2], Hui Du[2]
[1]Hangzhou Dianzi University, [2]Rice Microelectronics Co. Ltd.

5:30PM
P.15
Temperature-aware Thread Assignment of Many-core Processor
S. Xuan[1] and Y. Yang[2]
[1]Fudan University, [2]GPIX Inc

5:30PM
P.16
Separation of Concerns for Hardware Components of Embedded Systems in BIP
Maya Safieddine[1], Rouwaida Kanj[1], Fadi Zaraket[1], Ali Elzein[2], Mohamad Jaber[1]
[1]American University of Beirut, [2]IBM

5:30PM
P.17
Unreachable Code Identification For Improved Line Coverage
Luke Pierce and Spyros Tragoudas
Southern Illinois University

5:30PM
P.18
Efficient Task Partitioning and Scheduling for Thermal Management in Multicore Processors
Zhe Wang, Sanjay Ranka, Prabhat Mishra
University of Florida

SESSION 4A

Wednesday March 4, 2015

Challenges in SOC Design

Chair: **Steve Heinrich-Barna**, Texas Instruments
Co-Chair: **Charles Augustine**, Intel

10:20AM
4A.1
Fail-Safe I/O to Control RESET# Pin of DDR3 SDRAM and Achieve Ultra-Low System Power
Rajat Chauhan, Prajkta Vyavahare, Siva Kothamasu
Texas Instruments

10:40AM
4A.2
On-Line Reliability-Aware Dynamic Power Management for Real-Time Systems
Ming Fan[1], *Qiushi Han*[2], *Shuo Liu*[2], *Gang Quan*[2]
[1]Broadcom Corporation, [2]Florida International Unversity

11:00AM
4A.3
Design and Performance Parameters of an Ultra-Low Voltage, Single Supply 32bit Processor implemented in 28nm FDSOI Technology
Sylvain Clerc[1], *Fady Abouzeid*[1], *Darayus Adil Patel*[1], *Jean-Marc Daveau*[1], *Cyril Bottoni*[1], *Lorenzo Ciampolini*[1], *Fabien Giner*[1], *David Meyer*[1], *Robin Wilson*[1], *Philippe Roche*[1], *Sylvie Naudet*[1], *Arnaud Virazel*[2], *Alberto Bosio*[2], *Patrick Girard*[2]
[1]STMicroelectronics, [2]LIRMM

11:20AM
4A.4
Efficient Static D-Latch Standard Cell Characterization Using a Novel Setup Time Model
Arvind Sharma[1], *Yogendra Sharma*[2], *Sudeb Dasgupta*[1], *Anand Bulusu*[1]
[1]IIT Roorkee, [2]Synopsis India Pvt. Ltd.

11:40AM
4A.5
TDTB Error Detecting Latches: Timing Violation Sensitivity Analysis and Optimization
Matheus Moreira[1], *Dylan Hand*[2], *Ney Calazans*[1], *Peter Beerel*[2]
[1]PUCRS, [2]USC

SESSION 4B

Wednesday March 4, 2015

Network and Multiprocessing Systems

Chair: **Houman Houmayoun**, George Mason University
Co-Chair: **Lei Wang**, University of Connecticut

10:20AM
4B.1
Adaptive Mode Assignment in Performance-critical Cyber-physical Systems
zhaohui yuan, rong zhu, yiqing cao, guifen jiang
East China Jiaotong University

10:40AM
4B.2
Trading-Off System Load And Communication in Mapping Heuristics for Improving NoC-based MPSoCs Reliability
Marcelo Mandelli[1], Luciano Ost[2], Gilles Sassatelli[3], Fernando Moraes[1]
[1]PUCRS, [2]University of Leicester, [3]LIRMM

11:00AM
4B.3
2-Layer Laser Multiplexed Photonic Network-on-Chip
Dharanidhar Dang[1], Biplab Patra[1], Rabi N. Mahapatra[2]
[1]Graduate student, [2]Professor

11:20AM
4B.4
Exploring Shared Memory and Cache to Improve GPU Performance and Energy Efficiency
Hao Wen and Wei Zhang
Virginia Commonwealth University

11:40AM
4B.5
Enhancing Performance of Wireless NoCs with Distributed MAC Protocols
Karthi Duraisamy, Ryan Kim, Partha Pande
Washington State University

SESSION 4C

Wednesday March 4, 2015

Verification and Delay Measurement

Chair: **Vinod Viswanath**, Real Intent
Co-Chair: **Sreejit Chakravarty**, Intel Corporation

10:20AM
4C.1
Exploiting Abstraction, Learning from Random Simulation, and SVM Classification for Efficient Dynamic Prediction of Software Health Problems
Miroslav N. Velev[1], *Chaoqiang Zhang*[2], *Ping Gao*[1], *Alex D. Groce*[2]
[1]Aries Design Automation, [2]Oregon State University

10:40AM
4C.2
Optimum Domain Partitioning to Increase Functional Verification Coverage
Jomu George Mani Paret and Otmane Ait Mohamed
Concordia University

11:00AM
4C.3
Crosstalk-Aware Signal Probability-Based Dynamic Statistical Timing Analysis
Bao Liu[1], *Wenjun Wang*[1], *Yao Chen*[1], *Andrew Kahng*[2]
[1]UTSA, [2]UCSD

11:20AM
4C.4
A Low Area Calibration Technique of TDC Using Variable Clock Generator for Accurate On-Line Delay Measurement
Kentaroh Katoh[1] *and Kazuteru Namba*[2]
[1]National Institute of Technology, Tsuruoka College, [2]Chiba University

11:40AM
4C.5
Near Optimal Repair Rate Built-in Redundancy Analysis with Very Small Hardware Overhead
Woosung Lee, Keewon Cho, Jooyoung Kim, Sungho Kang
Department of Electrical & Electronic Engineering, Yonsei University, Seoul Korea

SESSION 5A

Wednesday March 4, 2015

Hardware and System Security

Chair: **Xuehui Zhang**, Oracle
Co-Chair: **Bao Liu**, University of Texas at San Antonio

1:00PM
5A.1
A Survey on Memristor Modeling and Security Applications
M. T. Arafin[1], C Dunbar[1], G. Qu[1], N. McDonald[2], L. Yan[2]
[1]University of Maryland, [2]Air Force Research Laboratory

1:20PM
5A.2
Digital PUF using Intentional Faults
Teng Xu and Miodrag Potkonjak
UCLA

1:40PM
5A.3
Side Channel Attacks in Embedded Systems: A Tale of Hostilities and Deterrence.
Jude Angelo Ambrose, Roshan G. Ragel, Darshana Jayasinghe, Tuo Li, Sri Parameswaran
The University of New South Wales

2:00PM
5A.4
Fault-Tolerant Methods for a New Lightweight Cipher Code SIMON
Jaya Dofe[1], Connor Reed[2], Ning Zhang[3], Qiaoyan Yu[1]
[1]University of New Hampshire, [2]Nashua North High School, [3]Xidian University

2:20PM
5A.5
Novel Self-Calibrating Recycling Sensor using Schmitt-Trigger and Voltage Boosting for Fine-Grained Detection
Cheng Wei Lin and Swaroop Ghosh
University of South Florida

2:40PM
5A.6
The Low Power Design of SM4 Cipher with Resistance to Differential Power Analysis
Yanbo Niu and Anping Jiang
Beijing Microelectronic Technology Institute

SESSION 5B

Wednesday March 4, 2015

Systems Implementation and Optimization

Chair: **Rajesh R. Berigei**, Texas Instruments, Inc.
Co-Chair: **Vivek Nandakumar**, Synopsys, Inc

1:00PM
5B.1
Comparative Evaluation of FPGA and ASIC Implementations of Bufferless and Buffered Routing Algorithms for On-Chip Networks
Yu Cai, Ken Mai, Onur Mutlu
Carnegie Mellon University

1:20PM
5B.2
Hardened Design Based on Advanced Orthogonal Latin Code against Two Adjacent Multiple Bit Upsets (MBUs) in Memories
Liyi Xiao, Jiaqiang Li, Jie Li, Jing Guo
Microelectronics Center, Harbin Institute of Technology, Harbin, 150001, China

1:40PM
5B.3
Scratch-Pad Memory Banking by Dynamic Programming for Embedded Data-Intensive Applications
Florin Balasa[1], Noha Abuaesh[1], Ilie I. Luican[2], Hongwei Zhu[3]
[1]American University in Cairo, Egypt, [2]Microsoft, USA, [3]ARM, USA

2:00PM
5B.4
A hypervisor approach with real-time support to the MIPS M5150 processor
Samir Zampiva, Carlos Moratelli, Fabiano Hessel
PUCRS

2:20PM
5B.5
RT-MIL-STD-1553+: Remote Terminal Controller for MIL-STD-1553B at 100-Mb/s Data Rate
Prateek Pendyala[1] and Vijaya Sankara Rao Pasupureddi[2]
[1]IIIT Hyderabad, [2]IIT Ropar

2:40PM
5B.6
Low Power Scheduling in High-level Synthesis using Dual-Vth Library
Samaneh Ghandali, Bijan Alizadeh, Zainalabedin Navabi
University of Tehran

SESSION 5C

Wednesday March 4, 2015

Packaging and 3D Integration

Chair: **Farhang Yazdani**, BroadPak
Co-Chair: **Paul Franzon**, NCSU

1:00PM
5C.1
A Novel Approach to IC, Package, and Board Co-Optimization
Gary Brist[1] and John Park[2]
[1]Intel, [2]Mentor Graphics

1:20PM
5C.2
An Effective Model for Evaluating Vertical Propagation Delay in TSV-based 3-D ICs
Masayuki Watanabe, Nanako Niioka, Rosely Karel, Tetsuya Kobayashi, Masa-aki Fukase, Masashi Imai, Atsushi Kurokawa
Hirosaki University

1:40PM
5C.3
Automatic Die Placement and Flexible I/O Assignment in 2.5D IC Design
Daniel Seemuth, Azadeh Davoodi, Katherine Morrow
University of Wisconsin - Madison

2:00PM
5C.4
Resource Allocation Methodology for Through Silicon Vias and Sleep Transistors in 3D ICs
Hailang Wang and Emre Salman
Stony Brook University

2:20PM
5C.5
Recovery of faulty TSVs in 3D ICs
Surajit Kumar Roy, Kaustav Roy, Chandan Giri, Hafizur Rahaman
Dept. of Information Technology, IIEST, Shibpur

2:40PM
5C.6
Novel Adaptive Power Gating Strategy of TSV-based Multi-layer 3D IC
Seungwon Kim, Seokhyeong Kang, Ki Jin Han, Youngmin Kim
Ulsan National Institute of Science and Technology, Republic of Korea

SESSION 6A

Wednesday March 4, 2015

Sensor Technology

Chair: **James Lei**, Ominvision
Co-Chair: **Xiaoning Qi**, Intel

3:20PM
6A.1
A Low-Power Field-Programmable Analog Array for Wireless Sensing
Brandon Rumberg and David Graham
West Virginia University

3:40PM
6A.2
On improving the range of inductive proximity sensors for avionic applications
Paul Leons[1], Aryan Yaghoubian[1], Glenn Cowan[1], Jelena Trajkovic[1], Yvon Nazon[2], Samar Abdi[1]
[1]Concordia University, [2]Thales, Canada

4:00PM
6A.3
A New Single Inductor Bipolar Multiple Output (SIBMO) Boost Converter Using Pulse Frequency Modulation (PFM) Control for OLED Drivers and Optical Transducers
Chun-Kai Chang[1], Chung-Hsin Su[2], Yung-Hua Kao[1], Ming-Hung Yu[1], Thilo Sauter[3], Paul Chao[1]
[1]Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan, [2]Sitronix Technology Corporation, [3]Center for Integrated Sensor Systems, Danube University Krems, Austria

4:20PM
6A.4
RFID Indoor Localization Based on Doppler Effect
Deivid Antunes Tesch, Everton Luís Berz, Fabiano Passuelo Hessel
PUCRS

4:40PM
6A.5
A Novel Physical Failure Analysis of MEMS Motion Sensor for Interface Inspection
Chunan Huang[1], Li Chuang[1], Kim Hsu[1], Steel Chung[2], Tim Chan[2]
[1]Integrated Service Technology, [2]Richtek Technology

SESSION 6B

Wednesday March 4, 2015

EDA for Design Exploration & Analysis Beyond Moore's Law

Chair: **Ofelya Manukyan**, Synopsys
Co-Chair: **Abishai Daniel**, Intel Corp.

3:20PM
6B.1
Exploring Memory Controller Configurations for Many-Core Systems with 3D Stacked DRAMs
Fen Ge[1], Jia Zhan[2], Yuan Xie[2], Vijaykrishnan Narayanan[3]
[1]Nanjing University of Aeronautics and Astronautics, China, [2]University of California at Santa Barbara, U.S.A., [3]The Pennsylvania State University, U.S.A.

3:40PM
6B.2
Virtual Logic Netlist: Enabling efficient RTL analysis
Spandana Rachamalla, Arun Joseph, Rahul Rao, Diwesh Pandey
IBM

4:00PM
6B.3
A Logic Difference Generator with Spare Cells Consideration for ECO Synthesis
Jui-Hung Hung[1], Yu-Cheng Lin[2], Wei-Kai Cheng[1], Tsai-Ming Hsieh[1]
[1]Chung Yuan University, [2]Kainan University

4:20PM
6B.4
Cells Reconfiguration Around Defects in CMOS/Nanofabric Circuits Using Simulated Evolution Heuristic
Abdalrahman M. Arafeh[1] and Sadiq M. Sait[2]
[1]University of British Columbia, [2]King Fahd University of Petroleum & Minerals

4:40PM
6B.5
Layout-aware Analog Synthesis Environment with Yield Consideration
Hsin-Ju Chang, Yen-Lung Chen, Conan Yeh, Chien-Nan Liu
National Central University

SESSION 6C

Wednesday March 4, 2015

Emerging Solid-State Device and Interconnect Technologies

Chair: **Paul Tong**, Pericom Semiconductor
Co-Chair: **Yiran Chen**, University of Pittsburg

3:20PM
6C.1
A Comparative Analysis of Symmetric and Asymmetric Dual-k spacer FinFETs from Device and Circuit Perspectives
Pankaj Pal, Brajesh Kaushik, Bulusu Anand, Sudeb Dasgupta
IIT Roorkee

3:40PM
6C.2
Technology/Circuit Co-optimization and benchmarking for Graphene Interconnects at Sub-10nm Technology Node
Chenyun Pan[1], Praveen Raghavan[2], Francky Catthoor[2], Zsolt Tokei[2], Azad Naeemi[1]
[1]Georgia Institute of Technology, [2]IMEC

4:00PM
6C.3
Domain Wall Motion based Low Power Hybrid Spin-CMOS 5-bit Flash Analog Data Converter
Karthik Yogendra, Mei-Chin Chen, Xuanyao Fong, Kaushik Roy
Purdue University

4:20PM
6C.4
6-T SRAM Performance Assessment with Stacked Silicon Nanowire MOSFETs
Ya-Chi Huang[1], Meng-Hsueh Chiang[2], Wei-Chou Hsu[2], Shiou-Ying Cheng[1]
[1]National Ilan University, [2]National Cheng Kung University

4:40PM
6C.5
Partially Depleted Silicon-on-Ferroelectric Insulator Field Effect Transistor (PD-SOFFET).
Azzedin Es-Sakhi and Masud Chowdhury
University of Missouri – Kansas City