Cyber-Physical systems
Security, IoT and Cy

Final Program

ISQED

2017
18th International Symposium on

QUALITY ELECTRONIC DESIGN

March 14-15, 2017
Santa Clara Convention Center,
Santa Clara, CA USA

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1ST CALL FOR PAPERS

ISQED 2018
19th International Symposium & Exhibits on
QUALITY ELECTRONIC DESIGN

March 2018
Santa Clara, CA, USA

ISQED Symposium 2018
www.ISQED.org

IEEE CAS EDS ReliabilitySociety ISQED

The International Symposium on Quality Electronic Design (ISQED) is the leading Electronic IC and System Design conference. ISQED emphasizes a holistic approach toward electronic design and intends to highlight and accelerate cooperation among the IC & System Design, IP providers, EDA, Semiconductor Process Technology and Manufacturing communities. ISQED spans two to three days, in three parallel tracks, hosting over 100 technical presentations, several keynote speakers, workshops/tutorials, special sessions, and other informal meetings. Past conference proceedings and papers have been published in the IEEE Xplore digital library and indexed by SCOPUS. For any question please contact the publication committee by sending email to isqed2018@isqed.org.

PAPERS ARE ACCEPTED IN THE FOLLOWING AREAS

A pioneer and leading multidisciplinary and Interdisciplinary conference, ISQED accepts and promotes papers in the following areas:

- ***IoT and Cyber-Physical systems***
- ***Cognitive Computing in Hardware***
- ***IP Design, quality, interoperability and reuse***
- ***Advanced 3D ICs & 3D Packaging***
- ***FPGA Architecture, Design, and CAD***
- ***Robust & Power-conscious Circuits & Systems***
- ***Advanced & 3D IC Packaging Technology***
- ***Hardware Security***
- ***PCB and PWB Technology & Manufacturing***
- ***Circuit & System Design***
- ***EDA Methodologies, Tools, Flows***
- ***Semiconductor & Nano Technology***
- ***Test & Verification***
- ***Design for Test and BIST***

SUBMISSION OF PAPERS

Paper submission must be done on-line through the conference web site at www.isqed.org. The guidelines for the final paper format are provided on the conference web site. In case of any problems send email to isqed2018@isqed.org. Please note the important dates shown below.

Important Deadlines

Submission Deadline	**Sept. 10, 2017**
Acceptance Notifications	December 5, 2017
Final Camera-Ready paper	January 10, 2018

WELCOME TO ISQED 2017

On behalf of the ISQED 2017 conference and technical committees, we are pleased to welcome you to the 18th International Symposium on Quality Electronic Design, ISQED 2017.

The 18th International Symposium on Quality Electronic Design (ISQED 2017) is the premier interdisciplinary and multidisciplinary electronic design conference aimed at bridging the gap among electronic/ semiconductor ecosystem members and providing electronic design tools, integrated circuit techniques, semiconductor manufacturing technologies, packaging technologies, and assembly and test methodologies to achieve design quality.

ISQED is held with the technical sponsorship of the IEEE Electron Devices Society, the IEEE Circuits and Systems Society, and the IEEE Reliability Society. ISQED continues to provide and foster a unique opportunity to participants to interact and engage themselves in cutting edge tutorials, presentations, and panel and plenary sessions.

We are happy to report a number of initiatives this year. The conference is organized around the theme "Security, IoT and Cyber-Physical Systems". We have invited two distinguished keynote speakers who will focus on these topics. Additionally, four embedded tutorials provide a holistic approach -- from devices to circuits to systems -- while covering state-of-the-art, in-depth studies in each of the topics impacting the quality of electronic design.

The two-day technical program with three parallel sessions packs around 100 papers highlighting the latest trends in electronic circuit and system design & automation, testing, verification, sensors, security, semiconductor technologies, cyber-physical systems, and cognitive computing. ISQED 2017 also features a panel discussion, entitled "Cybersecurity Challenges for the Automotive Industry" on Tuesday, March 14th.

All of the technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 14-15 at the Santa Clara Convention Center in Santa Clara, CA USA. Please refer to the conference booklet and/or ISQED website for program details.

We would like to thank the ISQED 2017 corporate sponsors: Synopsys, Mentor Graphics, Innovotek, and the Silicon Valley Polytechnic Institute for their valuable support of this conference. Welcome to another exciting year of ISQED! It couldn't have happened without your support and participation.

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ISQED 2017 Best Paper Candidates

1A.1

Electrical Modeling and Analysis of 3D Synaptic Array using Vertical RRAM Structure

Hongyu An[1], M. Amimul Ehsan[1] , Zhen Zhou[2], Yang Yi[1]

[1]Department of Electrical Engineering and Computer Science, University of Kansas, [2]Intel Corporation

1C.2

Variation-Immune Resistive Non-Volatile Memory using Self-Organized Sub-Bank Circuit Designs

Navid Khoshavi, Soheil Salehi, and Ronald F. DeMara

University of Central Florida

1C.3

Constructing Fast and Energy Ecient 1TnR based ReRAM Crossbar Memory

Lei Zhao[1], Lei Jiang[2], Youtao Zhang[1], Nong Xiao[3], and Jun Yang[1]

[1]University of Pittsburgh, [2]Indiana University Bloomington, [3]National University of Defense Technology

2A.1

Re-addressing SRAM Design and Measurement for Sub-Threshold Operation in View of Classic 6T vs. Standard Cell Based Implementations

Xin Fan[1], Jan Stuijt[1], Rui Wang[1,2], Bo Liu[1], and Tobias Gemmeke[1,3]

[1] Holst-Center / IMEC-nl, Eindhoven, The Netherlands, [2] ES, TU/e, Eindhoven, The Netherlands, [3] IDS, RWTH Aachen University, Germany

3B.1

Crossover Ring Oscillator PUF

Zihan Pang[1,2,3], Jiliang Zhang[2], Qiang Zhou[3], Shuqian Gong[2], Xu Qian[1], Bin Tang[4]

[1]School of Mechanical Electronic and Information Engineering, China University of Mining and Technology (Beijing), Beijing, China, [2]Software College, Northeastern University, Shenyang, China, [3]Department of Computer Science and Technology, Tsinghua University, China, [4]Guangdong Eshore Science and Technology Co., Ltd, Guangzhou, China

3C.1

Performance-Thermal Trade-offs for a VFI-Enabled 3D NoC Architecture

Dongjin Lee, Sourav Das, Partha Pratim Pande

School of EECS, Washington State University, Pullman, WA USA

4C.1

Performance Evaluation of Copper and Graphene Nanoribbons in 2-D NoC Structures

Ruturaj Pujari, Shaloo Rakheja

Department of Electrical and Computer Engineering, New York University

5A.1

Post-Fabrication Calibration of Near-Threshold Circuits for Energy Efficiency

Mohammad Saber Golanbari, Saman Kiamehr, Fabian Oboril, Anteneh Gebregiorgis, Mehdi B. Tahoori

Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany

ISQED 2017 Best Papers

2A.1

Re-addressing SRAM Design and Measurement for Sub-Threshold Operation in View of Classic 6T vs. Standard Cell Based Implementations

Xin Fan[1], Jan Stuijt[1], Rui Wang[1,2], Bo Liu[1], and Tobias Gemmeke[1,3]

[1] Holst-Center / IMEC-nl, Eindhoven, The Netherlands, [2] ES, TU/e, Eindhoven, The Netherlands, [3] IDS, RWTH Aachen University, Germany

3C.1

Performance-Thermal Trade-offs for a VFI-Enabled 3D NoC Architecture

Dongjin Lee, Sourav Das, Partha Pratim Pande

School of EECS, Washington State University, Pullman, WA USA

* Authors of best papers are honored during the Synopsys sponsored luncheon on Tuesday March 14

ISQED 2017 FELLOW AWARD

Paul Tong
Diodes Inc.

Paul Tong received both BSEE and MSEE from Columbia University in New York City, New York. He has been a DRAM & SRAM R&D Engineer at Micron and Samsung Semiconductor respectively and recently as the Senior Director of Technology at Pericom Semiconductor, which was acquired by Diodes Inc, in Nov., 2015.

Paul interests are in Novel Semiconductor Technologies, Device Physics and Device Reliability with special emphasis in On-Chip ESD protection designs. He is the holder of 10 US Patents and one International Patent.

Mr. Paul Tong is a Senior Member of the IEEE and has been an active and dedicated member of the ISQED technical committee for many years, and has made significant contributions to the quality of ISQED technical programs.

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ISQED 2017
GENERAL INFORMATION

March 14-15, 2017
Santa Clara Convention Center
5001 Great America Pkwy, Santa Clara, CA 95054

Embedded Tutorials

Chair:
Vinod Viswanath - *Real Intent*

Co-Chair:
Shiyan Hu - *Michigan Technological University*
Meeting Rooms 203-204

Tuesday, March 14, 1:45 PM - 2:45 PM

Accelerate DFT Verification to Reduce Test Costs, Close Coverage Gaps and Shorten Time to Market and Entitlement

Robert Serphillips
Mentor Graphics

Tuesday, March 14, 2:45 PM - 3:45 PM

Cyber-Physical Systems in Unmanned Aerial Vehicles

Dr. Huafeng Yu
Boeing Research & Technology

Wednesday, March 15, 1:00 PM - 2:00 PM

Design Automation for Cyber-Physical Systems: Challenges and Opportunities

Dr. Qi Zhu
University of California, Riverside

Wednesday, March 15, 2:00 PM - 3:00 PM

Computational Methods to Uncover Targeted Therapies for Cancer

Dr. Subarna Sinha
Stanford University

KEYNOTE SPEECHES

Tuesday, March 14, 9:00 AM - 10:10 AM
Meeting Rooms 203-204

Driverless Vehicles: Looking Ahead

Prof. Raj Rajkumar
George Westinghouse Professor
Carnegie Mellon University

Automotive, IoT Driving New Semiconductor IP and Compliance Requirements

Navraj Nandra
Sr. Director of Marketing
DesignWare Interface and Analog IP
Synopsys

Luncheon Panel Discussion

Tuesday, March 14, 12:30 PM - 1:30 PM
Meeting Rooms 203-204

Cybersecurity Challenges for Automotive Industry

Chair & Moderator
Prof. Gang Qu - *University of Maryland*

GENERAL INFORMATION

ISQED LUNCH & AWARDS CEREMONY

Tuesday, March 14, 11:55 AM - 12:30 PM
Meeting Rooms 203-204

ISQED Best Paper Awards

Recipients of the ISQED 2017 Best Paper Award will be recognized during the ISQED luncheon on Tuesday. List of best papers is shown in Page 3 of this document.

TECHNICAL SESSIONS

There are a total of 15 paper sessions held on Tuesday and Wednesday. Technical sessions are held in the format of three parallel tracks in **Meeting Rooms 201, 206 & 207**.

Poster Papers & Mixer

Poster display will take place on Tuesday afternoon 5:15 PM-6:45 PM in the Atrium area outside of the **Meeting Rooms.** Authors will be available to discuss their works and to answer questions. Refreshments will be served.

ON-SITE REGISTRATION

Tentative time schedule of on-site registration is as follows:

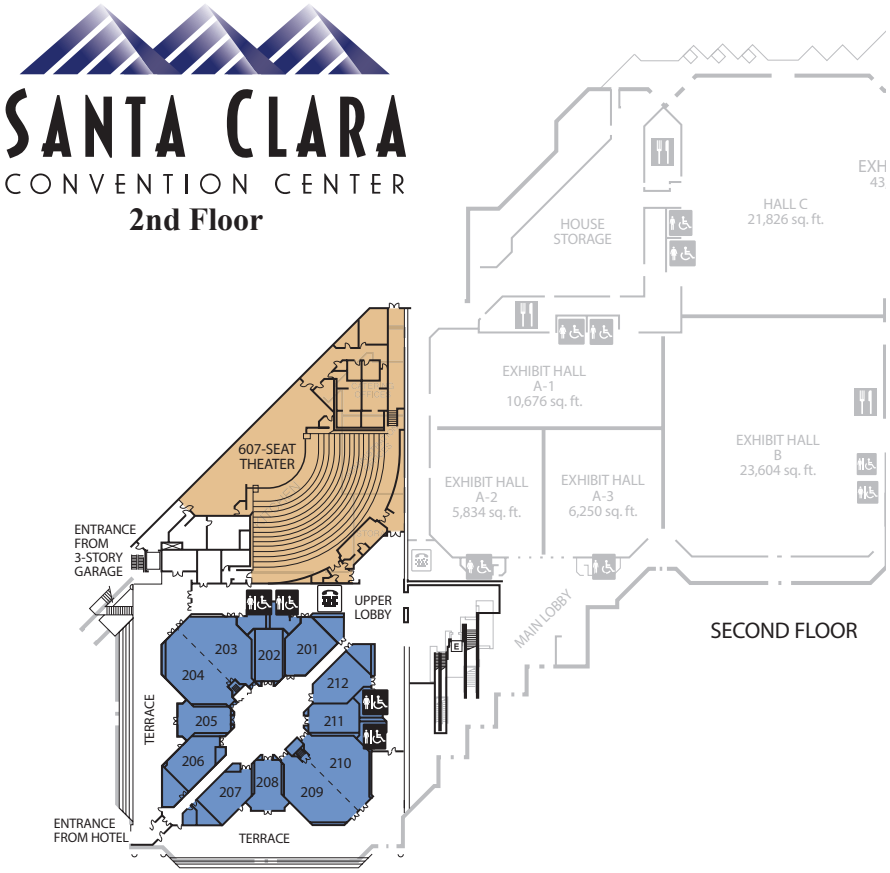
Tuesday, March 14	*8:00 AM - 4:00 PM*
Wednesday, March 16	*8:00 AM -1:00 PM*

Registration desk location will be beside the Meeting rooms 203/204.

Co-located Events

IoT Summit 2017
March 16-17
Meeting Rooms 203/204
www.IoT-Summit.org

FLOOR PLAN



Santa Clara Convention Center
2nd Floor
General Sessions & Tutorials:
Meeting Rooms 203/204

Breakout Rooms:
Meeting Rooms, 201, 206 and 207

PROGRAM AT A GLANCE

ISQED 2017 PROGRAM AT A GLANCE				
DATE	**TIME**			
TUESDAY 3/14/2017	*9:00 AM -10:10 AM*	**KEYNOTE SPEECHES** **(MEETING ROOMS 203/204)** **DRIVERLESS VEHICLES: LOOKING AHEAD** *RAJ RAJKUMAR - GEORGE WESTINGHOUSE PROFESSOR, CARNEGIE MELLON UNIVERSITY* **AUTOMOTIVE, IOT DRIVING NEW SEMICONDUCTOR IP AND COMPLIANCE REQUIREMENTS** *NAVRAJ NANDRA - SR. DIRECTOR OF MARKETING FOR THE DESIGNWARE INTERFACE AND ANALOG IP AT SYNOPSYS*		
	10:10 AM -10:25 AM	**MORNING BREAK**		
	10:25 AM -11:45 AM	**SESSION 1A** **COGNITIVE COMPUTING ON CONVENTIONAL AND EMERGING PLATFORMS** **MEETING ROOM 201**	**SESSION 1B** **(SPECIAL SESSION)** **DESIGN OPPORTUNITIES & CHALLENGES IN NON-VOLATILE TECHNOLOGIES** **MEETING ROOM 206**	**SESSION 1C** **A LOOK INTO FUTURE OF CIRCUITS, INTERCONNECTS AND MEMORY WITH EMERGING TECHNOLOGY** **MEETING ROOM 207**
	11:45 AM -11:55 AM	**BREAK**		
	11:55 AM -12:30 PM	**ISQED LUNCHEON & PANEL** **MEETING ROOMS 203/204** **BEST PAPER AWARDS , COMMITTEE RECOGNITION** SYNOPSYS® Accelerating Innovation		
	12:30 PM -1:30 PM	**PANEL DISCUSSION** **CYBERSECURITY CHALLENGES FOR AUTOMOTIVE INDUSTRY**		
	1:30 PM -1:45 PM	**BREAK**		
	1:45 PM -2:45 PM	**EMBEDDED TUTORIAL 1** **ACCELERATE DFT VERIFICATION TO REDUCE TEST COSTS, CLOSE COVERAGE GAPS AND SHORTEN TIME TO MARKET AND ENTITLEMENT** **MEETING ROOMS 203/204** Mentor Graphics®		
	2:45 PM -3:45 PM	**EMBEDDED TUTORIAL 2** **CYBER-PHYSICAL SYSTEMS IN UNMANNED AERIAL VEHICLES** **MEETING ROOMS 203/204**		
	3:45 PM -3:55 PM	**AFTERNOON BREAK**		
	3:55 PM -5:15 PM	**SESSION 2A** **LOW-POWER/FAULT-TOLERANT MEMORIES USING SCALED TECHNOLOGIES** **MEETING ROOM 201**	**SESSION 2B** **DESIGN FOR MANUFACTURABILITY AND RELIABILITY** **MEETING ROOM 206**	**SESSION 2C** **POSTER BRIEFS** **MEETING ROOM 207**
	5:15 PM -6:45 PM	**POSTER PAPERS & MIXER** **HALLWAY OUTSIDE MEETINGS ROOMS**		
WEDNESDAY 3/15/2017				
	9:00 AM -10:40 AM	**SESSION 3A** **POWER AND TIMING OPTIMIZATION** **MEETING ROOM 201**	**SESSION 3B** **HARDWARE SECURITY** **MEETING ROOM 206**	**SESSION 3C** **NOVEL RELIABILITY SOLUTIONS FOR 3D ICS** **MEETING ROOM 207**
	10:40 AM -10:50 AM	**MORNING BREAK**		
	10:50 AM -12:30 AM	**SESSION 4A** **(SPECIAL SESSION)** **LIGHTWEIGHT SECURITY FOR INTERNET-OF-THINGS: ATTACKS, COUNTERMEASURES AND EFFICIENT IMPLEMENTATIONS** **MEETING ROOM 201**	**SESSION 4B** **DESIGN FOR SMART SENSORS AND INTERNET OF THINGS** **MEETING ROOM 206**	**SESSION 4C** **INNOVATIVE ENERGY MANAGEMENT FOR MODERN SYSTEMS** **MEETING ROOM 207**
	12:30 PM -1:00 PM	**LUNCH BREAK**		
	1:00 PM -2:00 PM	**EMBEDDED TUTORIAL 3** **DESIGN AUTOMATION FOR CYBER-PHYSICAL SYSTEMS: CHALLENGES AND OPPORTUNITIES** **MEETING ROOMS 203/204**		
	2:00 PM -3:00 PM	**EMBEDDED TUTORIAL 4** **COMPUTATIONAL METHODS IN UNDERSTANDING CANCER BIOLOGY** **MEETING ROOMS 203/204**		
	3:00 PM -3:10 PM	**AFTERNOON BREAK**		
	3:10 PM -4:50 PM	**SESSION 5A** **ENERGY EFFICIENT LOGIC DESIGN USING SCALED TECHNOLOGIES** **MEETING ROOM 201**	**SESSION 5B** **SYNTHESIS AND RELIABILITY** **MEETING ROOM 206**	**SESSION 5C** **VERIFICATION AND TEST** **MEETING ROOM 207**

ISQED Keynote 1P.1

Tuesday March 14

9:00 AM - 9:35 AM
Meeting Rooms 203/204

Driverless Vehicles: Looking Ahead

Prof. Raj Rajkumar
Carnegie Mellon University

Self-driving vehicles seem to have become quite the rage in popular culture over just the past few years, triggered in good part by the DARPA Grand Challenges. Self-driving vehicles indeed hold the potential to revolutionize modern transportation. This talk will provide some insights on many basic questions that, need to be addressed for the revolution to take place in practice. What are the technological barriers that currently prevent vehicles to be driverless? What can or cannot be sensed or recognized? Can vehicles recognize and comprehend as good as, if not better than, humans? Does connectivity play a role? Will the technology be affordable only for the few? How do issues like liability, insurance, regulations and societal acceptance impact adoption? The talk will be based on road experiences and will add some speculation.

About Raj Rajkumar
Prof. Raj Rajkumar is the George Westinghouse Professor of Electrical & Computer Engineering and Robotics Institute at Carnegie Mellon University. At Carnegie Mellon, he directs the National University Transportation Center for Safety, which is sponsored by the US Department of Transportation. He also directs the Real-Time and Multimedia Systems Laboratory (RTML), and co-directs the General Motors-Carnegie Mellon Connected and Autonomous Driving Collaborative Research Laboratory (CAD-CRL). Raj has served as the Program Chair and General Chair of six international ACM/IEEE conferences on real-time systems, wireless sensor networks, cyber-physical systems and multimedia computing/networking. He has authored one book, edited another book, holds three US patents, and has more than 160 publications in peer-reviewed forums. Eight of these publications have received Best Paper Awards. He has given several keynotes and distinguished lectures at several international conferences and universities. He is an IEEE Fellow, an ACM Distinguished Engineer and a co-recipient of the IEEE Simon Ramo Medal. He has been given an Outstanding Technical Achievement and Leadership Award by the IEEE Technical Committee on Real-Time Systems. Prof Rajkumar's work has influenced many commercial operating systems. He was also the primary founder of Ottomatika Inc., a company that focused on delivering the core software intelligence for self-driving vehicles. Ottomatika was recently acquired by Delphi. His research interests include all aspects of cyber-physical systems.

Tuesday March 14

9:35 AM - 10:10 AM
Meeting Rooms 203/204

Automotive, IoT Driving New Semiconductor IP and Compliance Requirements

Navraj Nandra
Synopsys

The stringent design requirements for automotive and IoT system-on-chips is requiring the industry to adopt advanced process technologies such as 16-/14-nm and 7-nm to meet performance, power and area targets. Moving to these FinFET processes has significant implications on physical IP design. In addition, designers now have to meet functional and operational safety compliance for these automotive and IoT systems. Functional safety for IoT is typically categorized under IEC 61508. To meet the increasing demand for safety critical driver assistance systems, IP providers need to ensure that their products meet stringent automotive standards such as ISO 26262 functional safety, AEC-Q100 reliability testing and TS 16949 quality management. This presentation will discuss the technical specifications for automotive and IoT designs with respect to interface (USB, PCI Express, DDR) and foundation IP. This will include how Synopsys addresses the impact of aging/reliability such as HTOL, EM, TDDB, NBTI for physical IP on FinFET process technologies. The impact of the compliance requirements for these two market segments will also be presented for soft IP such as the addition of functional safety diagnostics.

About Navraj Nandra

Navraj Nandra is the Sr. Director of Marketing for the DesignWare Interface and Analog IP at Synopsys. He has worked in the semiconductor industry since the mid 80's as an analog/mixed signal IC designer for Philips Semiconductors, Austria Micro Systems, (San Jose & Austria) and EM-Marin (Switzerland). Navraj holds a masters degree in Microelectronics, majoring in analog IC design, from Brunel University and a post-graduate diploma in Process Technology from Middlesex University.

Panel Discussion

Tuesday March 14

12:30 PM –1:30 PM
Meeting Rooms 203/204

Cybersecurity Challenges for Automotive Industry

Chair & Moderator:
Prof. Gang Qu - University of Maryland

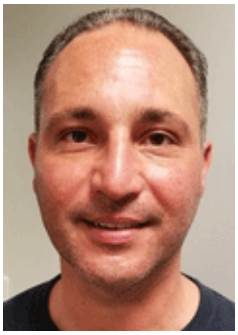
Summary:
Technology has changed the way we live. It is changing the way we drive too. In the past couple of years, we have witnessed one of the most dramatic transformations in automotive industry: vehicles are becoming intelligent and connected. They are not only a tool controlled by the so-called "drivers" to transport people and goods from one place to another. They are "talking" to each other as well as roadside infrastructure, making themselves autonomous or "driverless". In this panel, we have invited experts to share their views on cybersecurity challenges such as safety, security, and privacy that the automotive industry are facing. Our panelists will also discuss how our life will be changed (again) by the next generation vehicles.

Embedded Tutorial 1
Sponsored by Mentor Graphics

Tuesday March 14

1:45 PM - 2:45 PM
Meeting Rooms 203/204

Accelerate DFT Verification to Reduce Test Costs, Close Coverage Gaps and Shorten Time to Market and Entitlement



Robert Serphillips
Mentor Graphics

Summary: Traditional DFT process and methodologies are facing tremendous challenges to meet time to market goals and device coverage metrics. For a device to achieve high coverage, DFT engineers are faced with an exponentially increasing pattern set that leads to long pre-silicon simulation time and overall device test costs. Time to entitlement is at further risk exacerbating the need for a feature rich platform to accelerate traditional simulation processes and increase final test robustness. This presentation introduces emulation as the next logical step for DFT acceleration due to its ability to handle very large gate level designs with runtimes several orders of magnitude faster than the traditional software-based approach. This results in a higher quality design, yielding less silicon revisions, reduced lab costs and lower product and test costs.

About Robert Serphillips

Robert Serphillips has worked in the pre-silicon verification, post-silicon validation, and production design-for-test (DFT) fields. He has designed and debugged ATE test patterns on multiple stand alone and SoC devices spanning close to 20 years in the semiconductor industry. The products include a mix of consumer, automotive, industrial, military, networking and mixed-signal. Robert is currently a Technical Marketing Engineer with the Mentor Graphics Emulation Division.

Embedded Tutorial 2

Tuesday March 14

2:45 PM - 3:45 PM
Meeting Rooms 203/204

Cyber-Physical Systems in Unmanned Aerial Vehicles

Dr. Huafeng Yu
Boeing Research & Technology

Summary: Mobile autonomous systems, such as self-driving cars and unmanned aerial vehicles (UAVs), witness a very fast development recent years thanks to the maturity of artificial intelligence technologies and their supporting electronics. Because of less limitation in the design, production and application, remote-controlled or autonomous UAVs become the most deployed mobile autonomous systems in the world. UAVs generally feature limited size, weight, power, and range, but they are required to support expected level of performance, autonomy, reliability and safety. Design of UAVs under these limitations and requirements are still common issues. UAVs are cyber-physical systems (CPS), which are composed of hardware, software components as well as scheduling and resource allocation mechanisms. Based on this CPS point of view, in this tutorial, an overview of previous design issues and state-of-the-art solutions will be presented, particularly UAVs' system architecture and safety. Future design directions of UAV system architecture, coordination, security and safety will also be discussed.

About Huafeng Yu

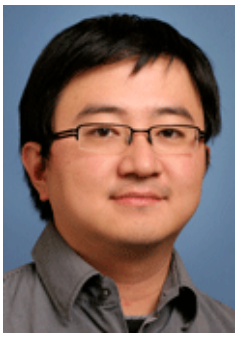
Huafeng Yu is a senior researcher with Boeing Research & Technology, located in Huntsville, Alabama. His main research interests are mainly in formal verification, model-based design, safety and reliability, cyber security, machine learning for mobile autonomous systems. He received his PhD from University of Lille 1 and Master's from University Joseph Fourier both in Computer Science in France. Huafeng is currently a member of IEEE Technical Committee on Cyber-Physical Systems (CCPS) and chair of its industry outreach committee. He is also a member of SAE standard committee for AADL. Huafeng serves as associate editor of IET Journal on Cyber-Physical Systems, as well as guest editor of IEEE Transaction on Sustainable Computing. He currently serves on program committee of DAC, DATE, ICCAD, SAC, etc.

Wednesday March 15

1:00 PM -2:00 PM

Meeting Rooms 203/204

Design Automation for Cyber-Physical Systems: Challenges and Opportunities



Dr. Qi Zhu

University of California, Riverside

Summary: Cyber-physical systems (CPS) such as autonomous and semi-autonomous vehicles, smart buildings, and industrial automation systems, are poised to bring immense economic and societal benefits. However, the design of these systems faces tremendous challenges from the rapid increase of system scale and heterogeneity, the close interaction with dynamic environment and human activities, the employment of multicore and distributed architectural platforms, and the stringent (and often conflicting) requirements on various design metrics. To address these challenges, it is critical to have a new set of design automation methods and tools for the modeling, synthesis and verification of cyber-physical systems. In this tutorial, I will discuss some of the unique challenges in CPS design, and introduce the design automation methods we developed for addressing them, including 1) a software architecture synthesis framework for generating correct, predictable and efficient software implementations from functional models, while optimizing metrics including control performance, schedulability, extensibility, fault tolerance, memory usage, modularity and reusability; 2) a cross-layer design framework for CPS security and its application in automotive electronic systems and vehicular networks; and 3) co-design and co-scheduling methodologies for energy-efficient building management and their integration with grid-level optimization.

About Qi Zhu

Dr. Qi Zhu is an Assistant Professor at the Department of Electrical and Computer Engineering in University of California, Riverside. Prior to joining UCR, he was a research scientist at the Strategic CAD Labs in Intel from 2008 to 2011. Dr. Zhu received a Ph.D. in EECS from University of California, Berkeley in 2008, and a B.E. in CS from Tsinghua University in 2003. His research interests include model-based design and software synthesis for cyber-physical systems, CPS security, energy-efficient buildings and infrastructures, and system-on-chip design. He received best paper awards at the Design Automation Conference (DAC) 2006, DAC 2007, International Conference on Cyber-Physical Systems (ICCPS) 2013, and ACM Transactions on Design Automation of Electronic Systems (TODAES) 2016. He received the National Science Foundation (NSF) CAREER award in 2016. Dr. Zhu has served on the technical program committees and as session organizer and chair for a number of international conferences, including DAC, ICCAD, DATE, ASP-DAC, CODES+ISSS, RTSS, RTAS, SAC, SIES, MEMOCODE, etc. He is the education committee chair of the IEEE Technical Committee on Cyber-Physical Systems. He received the ACM SIGDA Service Award in 2015.

Embedded Tutorial 4

Wednesday March 15

2:00 PM - 3:00 PM
Meeting Rooms 203/204

Computational Methods to Uncover Targeted Therapies for Cancer

Dr. Subarna Sinha
Stanford University

Summary: Cancer is a complex disease characterized by a large number of point mutations, large structural changes and epigenetic dysregulation. Cancer genome sequencing projects such as The Cancer Genome Altas (TCGA) have profiled tens of different tumor types with hundreds of samples per tumor type. These projects have demonstrated convincingly that cancer genomes exhibit considerable heterogeneity among different individuals. New analytical techniques are needed to extract common biological principles from massive amounts of data to provide useful mechanistic insights about cancer and thereby guide effective therapy.

In this tutorial, I will start with a brief overview of current methods to identify targeted therapies for cancer patients. Then, I will present Boolean implications, a new data mining method that can be used to mine large, heterogeneous cancer data sets and demonstrate its application to derive new actionable hypotheses for targeted therapy. I will describe MiSL (Mining Synthetic Lethals), a new Boolean implication-based method for mining synthetic lethal partners of recurrent cancer mutations by analyzing pan-cancer primary tumor data. Initial results are promising, and indicate that MiSL can effectively identify mutation- and cancer-specific pharmacologic targets and genetic biomarkers for tumor drug sensitivity.

About Subarna Sinha

Subarna Sinha is a Bioinformatics Program Leader at SRI International and a Research Scientist at Stanford University. Her research interests are in computational biology and data mining algorithms for biology, with an emphasis on cancer systems biology. Prior to that, she worked at research groups at Synopsys and at Intel, with a focus on Design-For-Manufacturability and logic synthesis. She received her PhD in EECS from UC Berkeley in 2002. She is the recipient of the Donald O Pederson best paper award in 2009 and the Synopsys Inventor of the Year award in 2009.

SESSION 1A

Tuesday March 14

Cognitive Computing on Conventional and Emerging Platforms

Chair: **Yang Yi**, University of Kansas
Co-Chair: **Hai (Helen) Li**, Duke University

10:25AM
1A.1
Electrical Modeling and Analysis of 3D Synaptic Array using Vertical RRAM Structure
Hongyu An[1], M. Amimul Ehsan[1], zhen zhou[2], Yang Yi[1]
[1]University of Kansas, [2]Intel Corporation

10:45AM
1A.2
SRAM Voltage Scaling for Energy-Efficient Convolutional Neural Networks
Lita Yang and Boris Murmann
Stanford University

11:05AM
1A.3
Stochastic-Based Multi-Stage Streaming Realization of Deep Convolutional Neural Network
Mohammed Alawad[1] and Mingjie Lin[2]
[1]PhD student at UCF, [2]University of Central Florida

11:25AM
1A.4
A Fast and Ultra Low Power Time-Based Spiking Neuromorphic Architecture for Embedded Applications
Tao Liu[1] and Wujie Wen[2]
[1]ECE Department, Florida International University, [2]Florida International University

SESSION 1B

Tuesday March 14

Design Opportunities and Challenges in Non-Volatile Technologies

Chair: **Sumeet Kumar Gupta**, Penn State University
Co-Chair: **Jack Sampson**, Penn State University

10:25AM
1B.1
Circuit Design for Beyond Von Neumann Applications Using Emerging Memory: From Nonvolatile Logics to Neuromorphic Computing
Meng-Fan (Marvin) Chang[1], Wei-Hao Chen[1], Win-San Khwa[1], Jun-Yi Li[1], Wei-Yu Lin[1], Huan-Ting Lin[1], Yongpan Liu[2], Yu Wang[2], Huaqiang Wu[2], Huazhong Yang[2]
[1]National Tsing Hua University, [2]Tsinghua University

10:45AM
1B.2
Harnessing Ferroelectrics for Non-volatile Memories and Logic
Sumeet Gupta[1], Danni Wang[2], Sumitha George[2], Ahmedullah Aziz[2], Xueqing Li[2], Suman Datta[3], Vijaykrishnan Narayanan[2]
[1]The Pennsylvania State University, [2]Penn State University, [3]University of Notre Dame

11:05AM
1B.3
Test Challenges in Embedded STT-MRAM Arrays
Insik Yoon and Arijit Raychowdhury
Georgia Institute of Technology

11:25AM
1B.4
Evaluating Tradeoffs in Granularity and Overheads in Supporting Nonvolatile Execution Semantics
Kaisheng Ma, Minli (Julie) Liao, Xueqing Li, Zhixuan Huan, John (Jack) Sampson
Penn State

SESSION 1C

Tuesday March 14

A Look into Future of Circuits, Interconnects and Memory with Emerging Technology

Chair: **Jayita Das**, Intel
Co-Chair: **Swatilekha Saha**, Cypress Semiconductor Corporation

10:25AM
1C.1
Communication Limits of On-Chip Graphene Plasmonic Interconnects
Shaloo Rakheja
New York University

10:45AM
1C.2
Variation-Immune Resistive Non-Volatile Memory using Self-Organized Sub-Bank Circuit Designs
Navid Khoshavi, Soheil Salehi, Ronald F. DeMara
University of Central Florida

11:05AM
1C.3
Constructing Fast and Energy Efficient 1TnR based ReRAM Crossbar Memory
Lei Zhao[1], Lei Jiang[2], Youtao Zhang[1], Nong Xiao[3], Jun Yang[1]
[1]University of Pittsburgh, [2]Indiana University Bloomington, [3]National University of Defense Technology

11:25AM
1C.4
Learning to Trust an Emerging Technology: The Molecular Field Coupling Nanocomputing Case Study
Mariagrazia Graziano[1], Ruiyu Wang[1], Marco Vacca[1], Fabrizio Riente[1], Giovanna Turvani[1], Franco Cacialli[2], Gianluca Piccinini[3]
[1]Politecnico di Torino, [2]University College London, [3]Politecnico di Torino, University College London

ISQED Luncheon & Panel Discussion

Tuesday March 14

11:55AM-1:30PM
Sponsored by Synopsys

11:55AM-12:30PM
Luncheon
Committee Recognition
Best Paper Awards

12:30PM-1:30PM
Panel Discussion

Cybersecurity Challenges for Automotive Industry

Chair & Moderator
Prof. Gang Qu
University of Maryland

Panelists
Anuja Sonalker - STEER Tech
Gaurav Bansal - Toyota InfoTechnology Center
Serge Leef – Mentor Graphics
Navraj Nandra - Synopsys

SESSION T12

Tuesday March 14

Embedded Tutorials 1 & 2

Chair: **Vinod Viswanath**, Real Intent
Co-Chair: **Shiyan Hu**, Michigan Technological University

1:45PM-2:45PM
Tutorial 1 (Sponsored by Mentor Graphics)

Accelerate DFT Verification to Reduce Test Costs, Close Coverage Gaps and Shorten Time to Market and Entitlement

Robert Serphillips
Mentor Graphics

2:45PM-3:45PM
Tutorial 2

Cyber-Physical Systems in Unmanned Aerial Vehicles

Dr. Huafeng Yu
Boeing Research & Technology

SESSION 2A

Tuesday March 14

Low-Power/Fault-Tolerant Memories Using Scaled Technologies

Chair: **Kurt Schwartz**, Texas Instruments, Inc.
Co-Chair: **Raviprakash Rao**, Texas Instruments, Inc.

3:55PM
2A.1
Re-addressing SRAM Design and Measurement for Sub-threshold Operation in View of Classic 6T vs. Standard Cell Based Implementations
Xin Fan[1], Jan Stuijt[1], Rui Wang[1], Bo Liu[1], Tobias Gemmeke[2]
[1]Holst-Centre / imec, [2]RWTH Aachen University

4:15PM
2A.2
Tunnel FET Based Ultra-Low-Leakage Compact 2T1C SRAM
Navneet Gupta[1], Adam Makosiej[2], Amara Amara[3], Andrei Vladimirescu[3], Costin Anghel[4]
[1]Institut supérieur d'électronique de Paris, France; LETI, Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA-LETI) France;, [2]LETI, Commissariat à l'énergie atomique et aux énergies alternatives (CEA-LETI) France, [3]Institut supérieur d'électronique de Paris, [4]ISEP

4:35PM
2A.3
Low Redundancy Matrix-Based codes for Adjacent Error Correction with Parity Sharing
Shanshan Liu, Liyi Xiao, Jie Li, Yihan Zhou, Zhigang Mao
Harbin Institute of Technology

4:55PM
2A.4
0.6 V operation, 16 % Faster Set/Reset ReRAM Boost Converter with Adaptive Buffer Voltage for ReRAM and NAND Flash Hybrid Solid-State Drives
Kota Tsurumi, Masahiro Tanaka, Ken Takeuchi
Chuo university

SESSION 2B

Tuesday March 14

Design for Manufacturability and Reliability

Chair: **Vivek Joshi**, GLOBALFOUNDRIES
Co-Chair: **Jayita Das**, INTEL

3:55PM
2B.1
Low Temperature Endurance Failures on Flash Memory
Steve Heinrich-Barna[1], Clyde Dunn[1], Douglas Verret[2]
[1]Texas Instruments, Inc, [2]Texas Instruments, Inc (Retired)

4:15PM
2B.2
Virtual Characterization for Exhaustive DFM Evaluation of Logic Cell Libraries
Samuel Pagliarini, Mayler Martins, Lawrence Pileggi
Carnegie Mellon University

4:35PM
2B.3
Overview and development of EDA tools for integration of DSA into patterning solutions
Andres Torres, Germain Fenger, Daman Khaira, Yuansheng Ma, Yuri Granik, Chris Kapral, Joydeep Mitra, Polina Krasnova
Mentor Graphics Corporation

4:55PM
2B.4
Performance- and Energy-Aware Optimization of BEOL Interconnect Stack Geometry in Advanced Technology Nodes
Kwangsoo Han, Andrew Kahng, Hyein Lee, Lutong Wang
UCSD

SESSION P & 2C*

Tuesday March 14

Posters

Chair: **Steve Heinrich-Barna**, Texas Instruments, Inc.
Co-Chair: **Vinod Viswanath**, Real Intent

5:15PM
P1
A Technique to Construct Global Routing Trees for Graphene Nanoribbon (GNR)
Subrata Das and Debesh Kumar Das
Jadavpur University

5:15PM
P2
Regularized Logistic Regression for Fast Importance Sampling Based SRAM Yield Analysis
Lama Shaer[1], Rouwaida Kanj[1], Rajiv Joshi[2], Maria Malik[3], Ali Chehab[1]
[1]American University of Beirut, [2]IBM, [3]George Mason University

5:15PM
P3
Binary Adder Circuit Design Using Emerging MIGFET Devices
Jeferson Baqueta, Felipe Marranghello, Augusto Neutzling, Vinicius Neves Possani, André Inacio Reis, Renato Perez Ribas
UFRGS

5:15PM
P4
A Case for Standard-Cell Based RAMs in Highly-Ported Superscalar Processor Structures
Sungkwan Ku[1], Elliott Forbes[2], Rangeen Basu Roy Chowdhury[3], Eric Rotenberg[4]
[1]North Carolina State University, [2]University of Wisconsin - La Crosse, [3]Intel, [4]North Carolina State University / Qualcomm

5:15PM
P5
Energy Efficient Analog Spiking Temporal Encoder with Verification and Recovery Scheme for Neuromorphic Computing Systems
Chenyuan Zhao, Jialing Li, Hongyu An, Yang Yi
University of Kansas

5:15PM
P6
3D-NOCET: A Tool for Implementing 3D-NoCs based on The Direct-Elevator Algorithm
maha Beheiry[1], Hassan Mostafa[2], Ahmed M. Soliman[2]
[1]Mentor Graphics, [2]Cairo University

5:15PM
P7
Design Technology Co-Optimization of Back End of Line Design Rules for a 7 nm Predictive Process Design Kit
Vinay Vashishtha, Ankita Dosi, Lovish Masand, Lawrence Clark
Arizona State University

5:15PM
P8
Investigation of Magnetic Field Attacks on Commercial Magneto-Resistive Random Access Memory
Alexander Holst[1], Jae-Won Jang[2], Swaroop Ghosh[2]
[1]University of South Florida, [2]Pennsylvania State University

5:15PM
P9
A 13T Radiation-Hardened Memory Cell for Low-Voltage Operation and Ultralow Power Space Applications
Chunhua Qi, Liyi Xiao, Mingxue Huo, Tianqi Wang, Rongsheng Zhang, Xuebing Cao
harbin institute of technology

5:15PM
P10
A New Approach for Selecting Inputs of Logic Functions During Debug
Amir Masoud Gharehbaghi[1] and Masahiro Fujita[2]
[1]The University of Tokyo, [2]University of Tokyo

5:15PM
P11
Fast and Energy-Aware Resource Provisioning and Task Scheduling for Cloud Systems
Hongjia Li[1], Ji Li[2], Wang Yao[3], Shahin Nazarian[2], Xue Lin[4], Yanzhi Wang[1]
[1]Syracuse University, [2]University of Southern California, [3]High School in China, [4]Northeastern University

5:15PM
P12
Evaluating the Benefits of a Relaxed BEOL Pitch for Deeply Scaled ICs
Mehmet M Isgenc, Samuel Pagliarini, Renzhi Liu, Larry Pileggi
Carnegie Mellon University

5:15PM
P13
STA Compatible Backend Design Flow for TSV-based 3-D ICs
Harry Kalargaris, Yi-Chung Chen, Vasilis Pavlidis
University of Manchester

5:15PM
P14
Off-Chip Test Architecture for Improving Multi-Site Testing Efficiency using Tri-State Decoder and 3V-Level Encoder
Sungyoul Seo[1], Hyeonchan Lim[1], Soyeon Kang[1], Sungho Kang[2]
[1]Yonsei University, Seoul, Korea, [2]Yonsei University

5:15PM
P15
Determining Proximal Geolocation of IoT Edge Devices via Covert Channel
Md Nazmul Islam, Vinay C Patil, Sandip Kundu
University of Massachusetts Amherst

*Session 2C consists of a 5min oral presentation of poster papers.

SESSION 3A

Wednesday March 15

Power and Timing Optimization

Chair: **Vinod Viswanath**, Real Intent
Co-Chair: **Anand Iyer**, Microsoft

09:00AM
3A.1
Clock tree optimization through selective airgap insertion
Daijoon Hyun, Wachirawit Ponghiran, Youngsoo Shin
KAIST

09:20AM
3A.2
An Analytical Model for Interdependent Setup/Hold-Time Characterization of Flip-flops
Hadi Ahmadi Balef, Hailong Jiao, José Pineda de Gyvez, Kees Goossens
Eindhoven University of Technology

09:40AM
3A.3
High Sigma Statistical Hold Time Analysis in FinFET Sequential Circuits
Sam Lo, Taylor Lee, Aaron Barker
Oracle

10:00AM
3A.4
Power Prediction of Embedded Scalar and Vector Processor: Challenges and Solutions
Vijay Kiran Kalyanam[1], Peter Sassone[2], Jacob Abraham[3]
[1]Qualcomm Technologies, Inc., [2]Qualcomm Technologies Inc., [3]CERC, The University of Texas at Austin

10:20AM
3A.5
Power-Delay Product Based Resource Library Construction for Effective Power Optimization in HLS
Shantanu Dutt[1] and Ouwen Shi[2]
[1]University of Illinois at Chicago, [2]Univ. of Illinois at Chicago

SESSION 3B

Wednesday March 15

Hardware Security

Chair: **Swaroop Ghosh**, Penn State University
Co-Chair: **Gang Qu**, University of Maryland

09:00AM
3B.1
Crossover Ring Oscillator PUF
Zihan Pang[1], Jiliang Zhang[2], Qiang Zhou[3], Shuqian Gong[2], Xu Qian[1], Bing Tang[4]
[1]China University of Mining & Technology (Beijing), [2]Northeastern University, China, [3]Tsinghua University, [4]Guangdong Eshore Science and Technology Co., Ltd

09:20AM
3B.2
Integrated Circuit Identification and True Random Numbers using 1.5-Transistor Flash Memory
Lawrence Clark, James Adams, Keith Holbert
Arizona State University

09:40AM
3B.3
Methodologies to Exploit ATPG Tools for De-camouflaging
Deepakreddy Vontela[1] and Swaroop Ghosh[2]*
[1]University of South florida, [2]Pennsylvania State University

10:00AM
3B.4
Low-Overhead Implementation of Logic Encryption Using Gate Replacement Techniques
Xiaoming Chen[1], Qiaoyi Liu[1], Yu Wang[1], Qiang Xu[2], Huazhong Yang[1]
[1]Tsinghua University, [2]The Chinese University of Hong Kong

10:20AM
3B.5
Scan Chain based IP Fingerprint and Identification
Xi Chen[1], Gang Qu[1], Aijiao Cui[2], Carson Dunbar[1]
[1]University of Maryland, [2]Harbin Institute of Technology Shenzhen Graduate School

SESSION 3C

Wednesday March 15

Novel Reliability Solutions for 3D ICs

Chair: **Payman Zarkesh-Ha**, University of New Mexico
Co-Chair: **Vivek Joshi**, GLOBALFOUNDRIES

09:00AM
3C.1
Performance-Thermal Trade-offs for a VFI-Enabled 3D NoC Architecture
Dongjin Lee, Sourav Das, Partha Pande
Washington State University

09:20AM
3C.2
A Legalization Algorithm for Multi-Tier Gate-Level Monolithic Three-Dimensional Integrated Circuits
Yiting Chen and Dae Hyun Kim
Washington State University

09:40AM
3C.3
Cooling Architectures using Thermal Sidewalls, Interchip Plates, and Bottom Plate for 3D ICs
Kaoru Furumi, Masashi Imai, Atsushi Kurokawa
Hirosaki University

10:00AM
3C.4
High Performance Virtual Channel Based Fully Adaptive Thermal-aware Routing for 3D NoC
Xin Jiang, Xiangyang Lei, Lian Zeng, Takahiro Watanabe
Graduate School of Information, Production & Systems, Waseda University

10:20AM
3C.5
Data Interface Buffer Compensation Scheme for Fast Calibration
Sameer Shekhar, Amit Kumar Jain, Pooja Nukala
Intel Corporation

SESSION 4A

Wednesday March 15

Lightweight Security for Internet-of-Things: Attacks, Countermeasures and Efficient Implementations

Chair: **Shivam Bhasin**, Nanyang Tech. University
Co-Chair: **Anupam Chattopadhyay**, Nanyang Tech. University

10:50AM
4A.1
Chosen-Input Side-Channel Analysis on Unrolled Light-Weight Cryptographic Hardware
Ville Yli-Mäyry, Naofumi Homma, Takafumi Aoki
Tohoku University

11:10AM
4A.2
An Electromagnetic Fault Injection Sensor using Hogge Phase-Detector
Wei He, Jakub Breier, Shivam Bhasin
Nanyang Technological University

11:30AM
4A.3
FPGA Implementation of Modeling Attack Resistant Arbiter PUF with Enhanced Reliability
Siarhei S. Zalivaka[1], Alexander A. Ivaniuk[2], Chip Hong Chang[1]
[1]Nanyang Technological University, [2]Belarusian State University of Informatics and Radioelectronics

11:50AM
4A.4
Towards Lightweight Identity-Based Encryption for the Post-Quantum-Secure Internet of Things
Tim Güneysu[1] and Tobias Oder[2]
[1]University of Bremen & DFKI, [2]Ruhr-Universität Bochum

12:10PM
4A.5
SHA-3 Implementation Using ReRAM based In-Memory Computing Architecture
Debjyoti Bhattacharjee, Vikramkumar Pudi, Anupam Chattopadhyay
Nanyang Technological University

SESSION 4B

Wednesday March 15

Design for Smart Sensors and Internet of Things

Chair: **Libor Rufer**, University Grenoble-Alpes, France
Co-Chair: **Kamesh Gadepally**, GigaCom Semiconductor

10:50AM
4B.1
A Hybrid RFID and CV System for Item-Level Localization of Stationary Objects
Everton Berz, Deivid Tesch, Fabiano Hessel
PUCRS University

11:10AM
4B.2
Energy Efficient Biopotential Acquisition Unit for Wearable Health Monitoring Applications
Wazir Singh, Yatharth Gupta, Paritosh Jivani, Sujay Deb
IIIT Delhi

11:30AM
4B.3
Wireless Charge Recovery System for Implanted Electroencephalography Applications in Mice
Leo Filippini[1], Diane Lim[2], Lunal Khuon[1], Baris Taskin[1]
[1]Drexel University, [2]University of Pennsylvania

11:50AM
4B.4
CAP: Configurable Resistive Associative Processor for Near-Data Computing
Mohsen Imani[1] and Tajana Rosing[2]
[1]University of California San Diego, [2]UCSD

12:10PM
4B.5
Low-power MEMS-based sensors
David Horsley
University of California, Davis

SESSION 4C

Wednesday March 15

Innovative Energy Management for Modern Systems

Chair: **Vivek Nandakumar**, Cadence Design Systems
Co-Chair: **Steve Heinrich-Barna**, Texas Instruments, Inc.

10:50AM
4C.1
Performance Evaluation of Copper and Graphene Nanoribbons in 2-D NoC Structures.
Ruturaj Pujari and Shaloo Rakheja
New York University

11:10AM
4C.2
Processor/Memory Co-scheduling Using Periodic Resource Server for Real-Time System Under Peak Temperature Constraints
Gustavo A. Chaparro-Baquero, Shi Sha, Soamar Homsi, Wujie Wen, Gang Quan
Florida International University

11:30AM
4C.3
Data Center Power Management for Regulation Service Using Neural Network-Based Power Prediction
Ning Liu[1], Xue Lin[2], Yanzhi Wang[1]
[1]Syracuse University, [2]Northeastern University

11:50AM
4C.4
An Energy Efficient Non-uniform Last Level Cache Architecture in 3D Chip-Multiprocessors
pooneh safayenikoo[1], Arghavan Asad[2], Mahmood Fathy[2], Farah Mohammadi[3]
[1]School of Computer Engineering, iran university of science and technology, [2]Iran University of Science and Technology, [3]Ryerson University

12:10PM
4C.5
Workload-Aware ASIC Flow for Lifetime Improvement of Multi-core IoT Processors
Scott Lerner and Baris Taskin
Drexel University

SESSION T34

Wednesday March 15

Embedded Tutorials 3 & 4

Chair: **Vinod Viswanath**, Real Intent
Co-Chair: **Shiyan Hu**, Michigan Technological University

1:00PM-2:00PM
Tutorial 3

Design Automation for Cyber-Physical Systems: Challenges and Opportunities

Dr. Qi Zhu
University of California, Riverside

2:00PM-3:00PM
Tutorial 4

Computational Methods to Uncover Targeted Therapies for Cancer

Dr. Subarna Sinha
Stanford University

SESSION 5A

Wednesday March 15

Energy Efficient Logic Design Using Scaled Technologies

Chair: **Kurt Schwartz**, Texas Instruments, Inc.
Co-Chair: **Raviprakash Rao**, Texas Instruments, Inc.

3:10PM
5A.1
Post-Fabrication Calibration of Near-Threshold Circuits for Energy Efficiency
Mohammad Saber Golanbari[1], Saman Kiamehr[2], Fabian Oboril[1], Anteneh Gebregiorgis[1], Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology, [2]Karlsruhe Institute of Technology (KIT)

3:30PM
5A.2
Composite Spintronic Accuracy-Configurable Adder for Low Power Digital Signal Processing
Shaahin Angizi[1], Zhezhi He[2], Ronald F. DeMara[3], Deliang Fan[3]
[1]Department of Electrical and Computer Engineering, University of Central Florida, [2]Department of ECE, University of Central Florida, [3]University of Central Florida

3:50PM
5A.3
Low Latency Divider using Ensemble of Moving Average Curves
Yuhan Fu, Masayuki Ikebe, Takeshi Shimada, Tetsuya Asai, Masato Motomura
Hokkaido University

4:10PM
5A.4
Adder Implementation in Reconfigurable Resistive Switching Crossbar
Pravin Mane, Sudeep Mishra, Ravish Deliwala, Ramesha C. K.
BITS Pilani K K Birla Goa Campus

4:30PM
5A.5
High precision yet wide range on-chip oscillator with dual charge-discharge technique
Abhijit Das[1] and Joonsung Park[2]
[1]Texas Instruments, [2]Texas Instruments, Inc.

SESSION 5B

Wednesday March 15

Synthesis and Reliability

Chair: **Srini Krishnamoorthy**, Advanced Micro Devices Inc.
Co-Chair: **Dae Hyun Kim**, Washington State University

3:10PM
5B.1
In&Out: Restructuring for Threshold Logic Network Optimization
Chia-Chun Lin[1], Chiao-Wei Huang[1], Chun-Yao Wang[1], Yung-Chih Chen[2]
[1]Department of Computer Science, National Tsing Hua University, [2]Department of Computer Science & Engineering, Yuan Ze University

3:30PM
5B.2
Systematic Approximate Logic Optimization using Don't Care Conditions
Sahand Salamat[1], Mehrnaz Ahmadi[1], Bijan Alizadeh[1], Masahiro Fujita[2]
[1]University of Tehran, [2]University of Tokyo

3:50PM
5B.3
Comparative Study of Path Selection and Objective Function in Replacing NBTI Mitigation Logic
Shumpei Morita, Song Bian, Michihiro Shintani, Masayuki Hiromoto, Takashi Sato
Kyoto University

4:10PM
5B.4
Methods for equivalence checking and ECO support under C-based design through reproduction of C descriptions from implementation designs
Qinhao Wang, Yusuke Kimura, Masahiro Fujita
University of Tokyo

4:30PM
5B.5
On Quality in Experimental Evaluation
Jan Schmidt
Czech Technical University in Prague

SESSION 5C

Wednesday March 15

Verification and Test

Chair: **Vinod Viswanath**, Real Intent
Co-Chair: **Sreejit Chakravarty**, Intel

3:10PM
5C.1
Cost-Quality Trade-offs of Approximate Memory Repair Mechanisms for Image Data
Qianqian Fan, Sachin Sapatnekar, David Lilja
University of Minnesota

3:30PM
5C.2
Aging-aware critical paths for process related validation in the presence of NBTI
phaninder alladi[1] and Spyros Tragoudas[2]
[1]southern illinois university, [2]Southern Illinois University Carbondale

3:50PM
5C.3
Broadcast Scan Compression Based on Deterministic Pattern Generation Algorithm
Hyeonchan Lim, Sungyoul Seo, Soyeon Kang, Sungho Kang
Yonsei University

4:10PM
5C.4
Wordline overdriving test: An effective predictive testing method for SRAMs against BTI aging
Jizhe Zhang[1] and Sandeep Gupta[2]
[1]Electrical Engineering Department, University of Southern California, [2]University of Southern California (USC)

4:30PM
5C.5
Failures and Verification Solutions Related to Untimed Paths in SOCs
Pranav Ashar[1], Vikas Sachdeva[2], Vinod Viswanath[2]
[1]Real Intent, Inc, [2]Real Intent, Inc.