ISQED’21 Paper Submission Deadline Oct. 2

Symposium on Quality Electronic Design (ISQED) is announcing the paper submission deadline for the 2021 event. The conference is planned for April 2021.

ISQED'21 Call for Papers

ISQED'21

SANTA CLARA, CA, USA, September 22, 2020 /EINPresswire.com/ -- ISQED’21 Call for Papers- Deadline Oct. 2
21st International Symposium on Quality Electronic Design
April 7-8, 2021
Santa Clara, CA
The conference theme is AI in Electronic Design, Quantum Computing, Hardware Security, 3D Integration, and IoT
https://www.isqed.org/English/Conference/Call_for_Papers.html

Symposium on Quality Electronic Design (ISQED) is announcing the paper submission deadline for 2021 event. ISQED is an internationally reputable conference, sponsored by IEEE CASS, IEEE EDS, and IEEE Reliability Societies, and in cooperation with ACM/SigDA. To be considered for presentation and publication by IEEE, authors are asked to send their articles before Oct. 2, 2020. The conference is planned to be held on April 2021 in Santa Clara, CA, USA. The final format will be announced later when the COVID-19 situation becomes clear.

A partial list of topics of interest includes:

Hardware and System Security

Attacks and countermeasures including but not limited to side-channel attacks, reverse engineering, tampering, and Trojans
Hardware-based security primitives including PUFs, TRNGs, and ciphers
Security, privacy, trust protocols, and trusted information flow
Ensuring trust using untrusted tools, IP, models, and manufacturing
Secure hardware architectures Secure memory systems

Post-quantum security primitives
Security challenges and opportunities of emerging nanoscale devices
IoT and cyber-physical system security
Any other topics related to hardware security

Electronic Design Automation Tools and Methodologies

EDA and physical design tools, processes, methodologies, and flows
Design tools for analysis/ tolerance of variation, aging, and soft-errors
Design and maintenance of hard and soft IP blocks
Challenges and solutions of integrating, testing, qualifying and manufacturing IP blocks from multiple vendors
EDA for non-traditional problems such as smart power grid and solar energy
EDA tools and methodologies for 3D integrations, and advanced packaging
Modeling and Simulation of Semiconductor Processes and Devices (TCAD)
CAD for bio-inspired and neuromorphic systems
EDA tools, methodologies and applications for Photonics devices, circuit and system design
EDA for MEMS Any other topics related design automation tools and methodologies

Design Test and Verification

Hardware and software formal-, assertion-, and simulation-based design verification techniques
All areas of DFT, ATE and BIST for digital designs, analog/mixed-signal IC's, SoC's, and memories
Test synthesis and synthesis for testability
Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction
SoC/IP testing strategies Design methodologies dealing with the link between testability and manufacturing
Hardware/software co-verification
Advanced methodologies, test-benches, and flows (e.g., UVM, HDLs, HVLs)
Formal and semi-formal verification and validation techniques
Safety and security in verification and validation New methods and tools supporting functional safety and security
Self-checking test-benches in analog verification
Any other topics related to design test and verification

Emerging Device and Process Technologies and Applications

Design, simulation and modeling of emerging technologies
Design, simulation and modeling of emerging non-volatile memory and logic, such as STT-RAM, PC-RAM, R-RAM, and Memristors
Application of emerging devices for storage and computation including but not limited to

cognitive, neuromorphic, or quantum computing
Qubit technologies and quantum computing Specialty technologies such as MEMs, NEMs
Novel or emerging solid state nano-electronic devices and concepts
Design and Technology Co-Optimization
Optimization-based methodologies that address the interaction between design (custom, semi-custom, ASIC, FPGA, RF, memory, etc.)
Advanced-node manufacturing techniques such as multiple patterning, EUV lithography, DSA lithography,
Advanced interconnect (e.g., air gap for local interconnect, Si photonics, etc.).
Modeling, analysis, and optimization of technology implications on performance metrics like power consumption, timing, area, and cost.
Design methods and tools to improve yield and manufacturability.
Any other topics related to emerging device technologies and applications

Circuit Design, 3D Integration and Advanced Packaging

Low power, high-performance, and robust design of logic, memory, analog, interconnect, RF, programmable logic, and FPGA circuits
Techniques for leakage control, power optimization, and power management
Analog circuit design including but not limited to all-digital PLLs and DLLs, ADC's and DAC's
Adaptive and resilient digital circuits and systems
On-chip process, voltage, temperature, and aging sensors and monitoring
Hardware design for IoT sensors and actuators including digital logic, memory design, wireless communications, energy harvesting, signal processing, and power management
Innovative packaging technologies including 3D IC, 2.5D or interposer, and multi-chip module and their impact on design
Design techniques, methodologies and flows for vertically integrated circuits/chips
Modeling and mitigation of device interactions for 3D ICs
Design of die-to-die interfaces in 3D/2.5D ICs
Design-for-testability and system-level design issues in 3D/2.5D
Die-package co-design
Any other topics related to circuit design, 3D integration and advanced packaging

System-level Design and Methodologies
Methods and tools aiming at quality of systems including multi-core processors, graphics processors embedded systems, SoC, novel accelerator designs, and heterogeneous architecture designs
System-level trade-off analysis and multi-objective (e.g. yield, power, delay, area, etc.) optimization
System level power and thermal management
Exploration of influence of emerging technologies on the system level design
System level modeling and simulation to characterize effects of process, voltage, temperature, and aging on power, performance, and reliability

Cyber-Physical Systems – Design, Methodologies & Tools
HW/SW co-design, co-simulation, co-optimization, and co-exploration
HW/SW prototyping and emulation on FPGAs
Micro-architectural transformation
System communication architecture
Application driven heterogeneous computing platforms
Network-on-chip design methodologies
Any other topics related to system level design and methodologies

Cognitive Computing Hardware

Neuromorphic computing and non-Von Neumann architectures
Hardware and architecture for neural networks and system-level design for (deep) neural computing Neural network acceleration techniques including GPGPU, FPGA and dedicated ASICs
Safe and secure machine learning Hardware accelerators for Artificial Intelligence Cognitive-inspired computing fundamentals
Cognitive-inspired computing systems
Cognitive-inspired computing with big data
Cognitive-inspired intelligent interaction AI-assisted cognitive computing approaches
Brain analysis for cognitive-inspired computing Internet of cognitive Things
Cognitive environment, sensing and data
Cognitive robots and agents Security issue in cognitive-inspired computing
Test-bed, prototype implementation and applications
Any other topics related to cognitive computing hardware

Submission of Papers (Regular, WIP, Special Sessions)
For any information about submission process refer to:
https://www.isqed.org/English/Conference/Call_for_Papers.html

About ISQED

ISQED is the premier interdisciplinary and multidisciplinary conference, being held with the technical sponsorship of IEEE CASS, EDS, and Reliability Society. All past Conference proceedings & Papers have been published in IEEE Xplore digital library and indexed by Scopus.
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